# 18+1 Channel Voltage Buffers for TFT LCD

## Introduction

### General Description

The EC5579 is a 18+1 channel voltage buffers that buffers reference voltage for gamma correction in a thin film transistor liquid crystal display (TFT LCD). This device incorporating a Vcom amplifier circuits, four rail to rail buffer amplifier circuits (the highest two stage and lowest two stage) and 14 buffer amplifiers circuits.

The EC5579 is available in a space saving 48-pin TQFP package, and the operating temperature is from –20°C to +85°C.
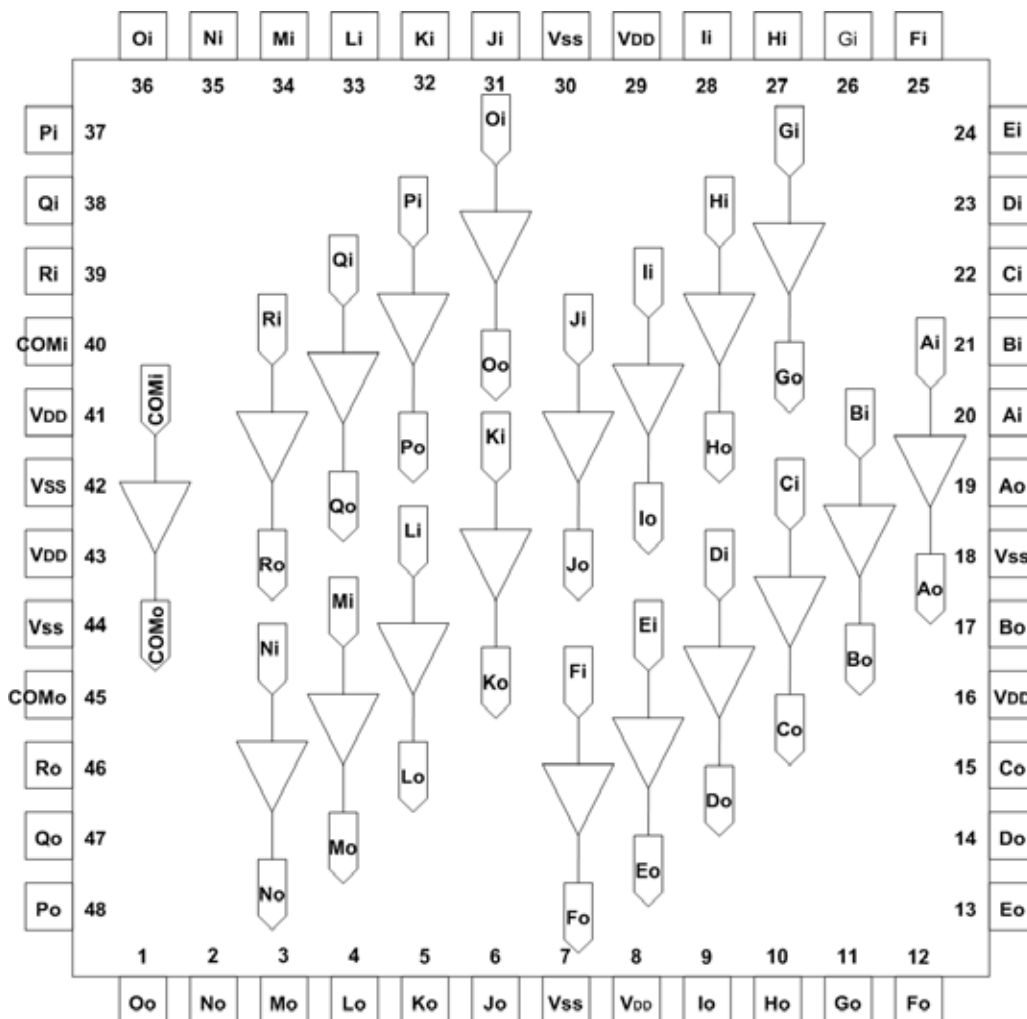
## Features

- Wide supply voltage range 6.5V ~ 18V
- Rail-to-rail output swing (The highest two stage & lowest two stage)
- High slew rate 1V/μ s
- GBWP 1 MHz
- 2 MHz -3dB Bandwidth
- Large Vcom Drive Current: ±100mA(Max)
- Ultra-small Package TQFP-48

## Applications

- TFT-LCD Reference Driver

## Pin Configuration



**A,B,Q,R: Rail to Rail OPAMPs**

## Ordering/Marking Information

| Package | Part Number | Marking | Marking Information |
|---|---|---|---|
| TQFP 48 | EC5579-F | AS19-F | Lead free |
| | EC5579-G | AS19-G | Green Mode |
| | EC5579-HF | AS19-HF | Lead free with exposed pad (3.05x3.05 mm) |
| | EC5579-HG | AS19-HG | Green Mode with exposed pad (3.05x3.05 mm) |
| | EC5579E-H1F | AS19-H1F | Lead free with exposed pad (5.0x5.0 mm) |
| | EC5579E-H1G | AS19-H1G | Green Mode with exposed pad (5.0x5.0 mm) |

## Ordering Information

EC5579 X - X X

F: Lead-Free
G: Green Mode

H: Exposed pad (3.05x3.05 mm)
H1: Exposed pad (5.0x5.0 mm)

E: Package type : TQFP48
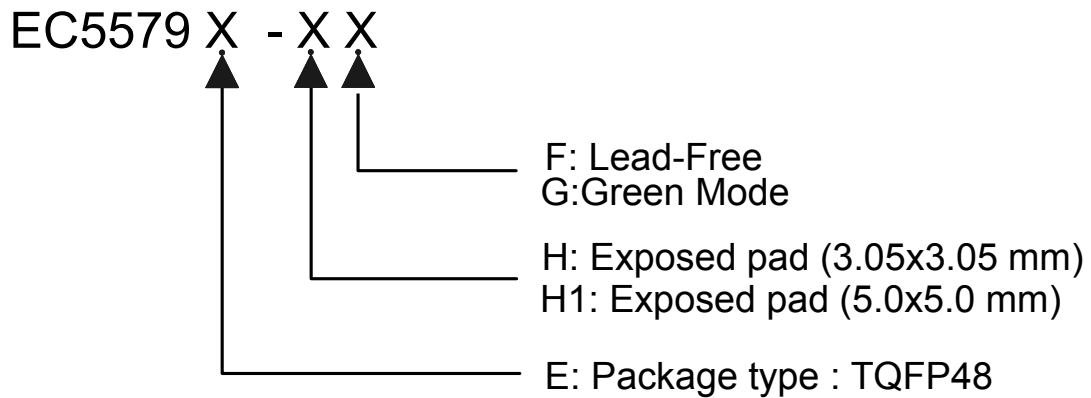
## Package Marking Indication

AS19-XX
Date Code
Lot. Number
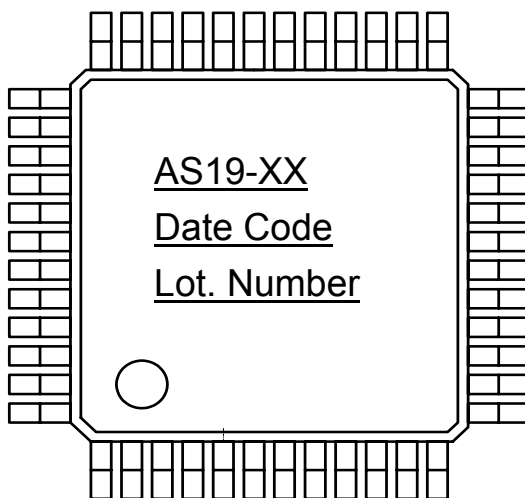
## Absolute Maximum Ratings (TA=25°C)

Values beyond absolute maximum ratings may cause permanent damage to the device. These are stress ratings only; functional device operation is not implied. Exposure to AMR conditions for extended periods may affect device reliability.

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage between $V_{S+}$ and $V_{S-}$ | Vs | +18 | V |
| Input Voltage | — | $V_{S-}$ -0.5 | V |
| (For rail to rail) | — | $V_{S+}$ +0.5 | V |
| Maximum Output Current (A ~ R Buffers) | Iout | ±30 | mA |
| Maximum Output Current (Com Buffer) | Iout(com) | ±100 | mA |
| Maximum junction Temperature | $T_J$ | +150 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 to +150 | °C |
| Operating Temperature Range | $T_{OP}$ | -20 to +85 | °C |
| Lead temperature | $T_{lead}$ | 260 | °C |
| ESD Voltage | — | 2 | KV |

Important Note:

All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only.

Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

## Electrical Characteristics

$V_{S+}$= +5V, $V_{S-}$ = -5V, $R_L$ = 10kΩ and $C_L$ = 10pF to 0V, $T_A$ = 25°C unless otherwise specified.

| Parameter | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Input Characteristics** | | | | | | |
| $V_{OS}$ | Input Offset Voltage | $V_{CM}$= 0V | — | 2 | 12 | mV |
| $TCV_{OS}$ | Average Offset Voltage Drift | [1] | — | 5 | — | µV/°C |
| $I_B$ | Input Bias Current | $V_{CM}$= 0V | — | 2 | 50 | nA |
| $R_{IN}$ | Input Impedance | — | — | 1 | — | G |
| $C_{IN}$ | Input Capacitance | — | — | 1.35 | — | pF |
| **Output Characteristics** | | | | | | |
| $V_{OL}$ | Output Swing Low | $I_L$= -5mA (A, B, Q, R rail-to-rail Buffers) | | -4.92 | -4.85 | V |
| $V_{OH}$ | Output Swing High | $I_L$= 5mA (A, B, Q, R rail-to-rail Buffers) | 4.85 | 4.92 | — | V |
| $V_{OL}$ | Output Swing Low | $I_L$= -5mA (C ~ P Buffers) | -3.5 | — | — | V |
| $V_{OH}$ | Output Swing High | $I_L$= 5mA (C ~ P Buffers) | 3.5 | — | — | V |
| $I_{SC}$ | Short Circuit Current | (A ~ R Buffers) | — | ±120 | — | mA |
| $I_{OUT}$ | Output Current | (A ~ R Buffers) | — | ±30 | — | mA |
| $I_{SC(Com)}$ | Short Circuit Current | (Com Buffer) | — | ±300 | — | mA |
| $I_{OUT(Com)}$ | Output Current | (Com Buffer) | — | ±100 | — | mA |
| **Power Supply Performance** | | | | | | |
| PSRR | Power Supply Rejection Ratio | $V_S$ is moved from ±3.25V to ±7.75V | 60 | 80 | — | dB |
| $I_S$ | Supply Current (Per Amplifier) | No Load (A ~ R Buffers) | — | 500 | 750 | µA |
| $I_{S(Com)}$ | Supply Current | (Com Buffer) | — | 8 | — | mA |
| **Dynamic Performance** | | | | | | |
| SR | Slew Rate [2] | -4.0V  $V_{OUT}$  4.0V, 20% to 80% | — | 1 | — | V/µs |
| $t_S$ | Settling to +0.1% (AV = +1) | (AV = +1), $V_O$=2V Step | — | 5 | — | µs |
| BW | -3dB Bandwidth | RL = 10K , CL = 10PF | — | 2 | — | MHz |
| PM | Phase Margin | RL = 10K , CL = 10PF | — | 60 | — | Degrees |
| CS | Channel Separation | f = 1 MHz | — | 75 | — | dB |

1. Measured over operating temperature range

2. Slew rate is measured on rising and falling edges

**18+1 Channel Voltage Buffers for TFT LCD**

## Typical Performance Characteristics
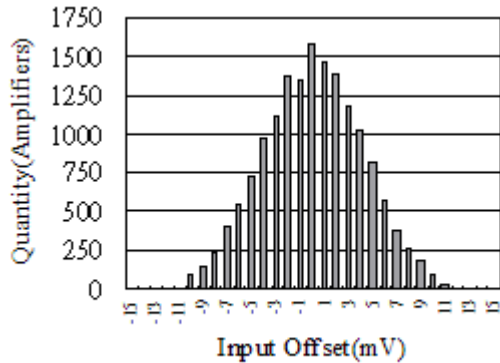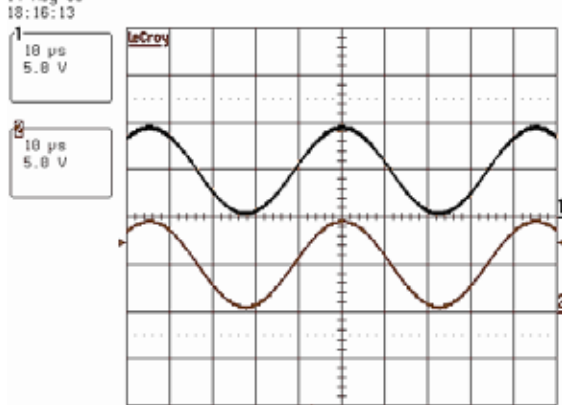
VCC = 10V, F: 10K
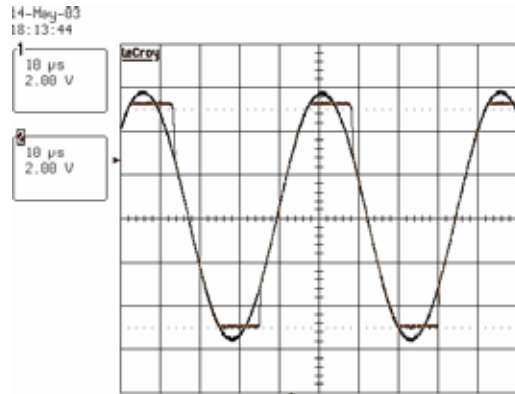
VCC = 10V, F: 10K

VCC = 10V, F: 1K
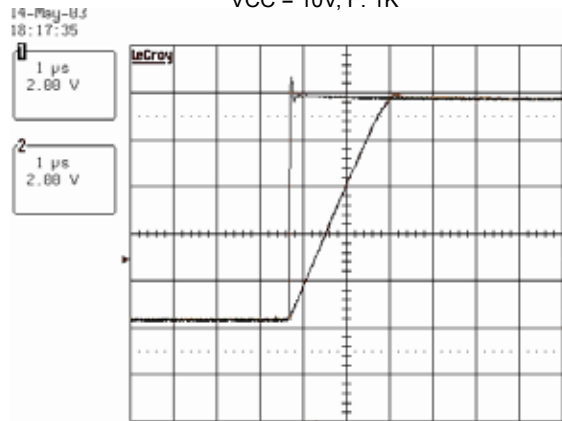
Figure3. Rail to Rail Capability
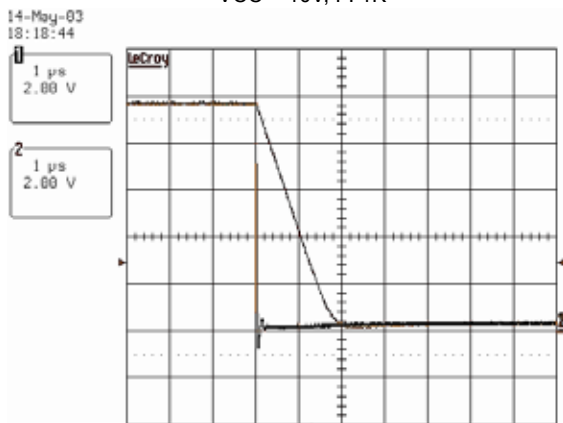
Figure4. Large Signal Transient Response

VCC = 10V, F: 1K

VCC = 10V, F: 1K

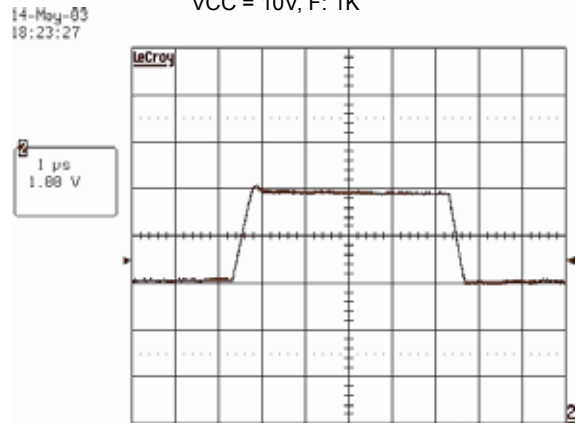Figure5. Large Signal Transient Response

Figure6. Small Signal Transient Response

**18+1 Channel Voltage Buffers for TFT LCD**
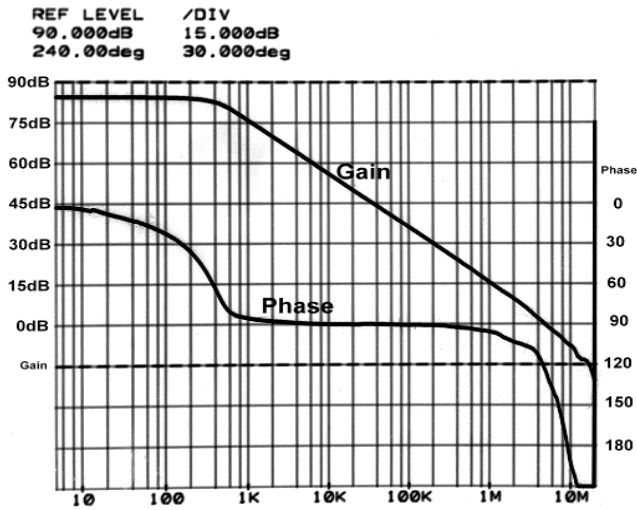
## Typical Performance Characteristics (Continued)
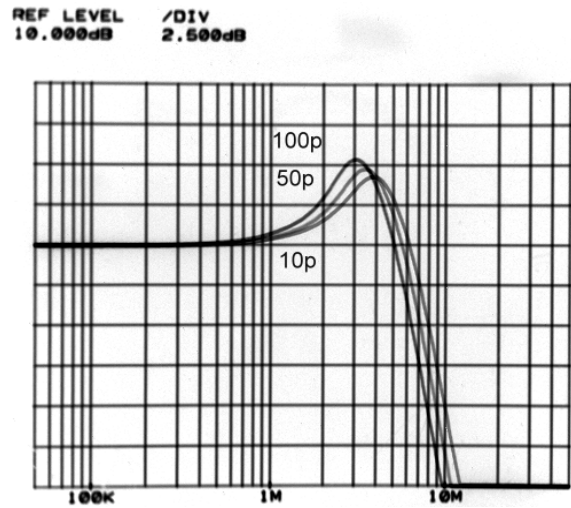


Figure7. Open Loop Gain & Phase vs. Frequency
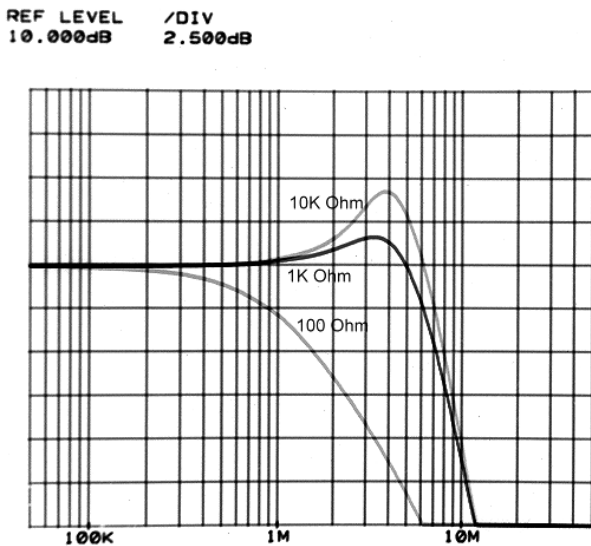


Figure8. Frequency Response for Various $C_L$



Figure9. Frequency Response for Various $R_L$

## Applications Information

### Product Description

The EC5579 rail-to-rail quad channels amplifier is built on an advanced high voltage CMOS process. It's beyond rails input capability and full swing of output range made itself an ideal amplifier for use in a wide range of general-purpose applications. The features of 1µS high slew rate, fast settling time, 2MHz of GBWP as well as high output driving capability have proven the EC5579 a good voltage reference buffer in TFT-LCD for grayscale reference applications. High phase margin and extremely low power consumption (500µA per amplifier) make the EC5579 ideal for Connected in voltage follower mode for low power high drive applications

### Supply Voltage, Input Range and Output Swing

The EC5579 can be operated with a single nominal wide supply voltage ranging from 6.5V to 18V with stable performance over operating temperatures of -20 °C to +85 °C.

With 500mV greater than rail-to-rail input common mode voltage range and 75dB of Common Mode Rejection Ratio, the EC5579 allows a wide range sensing among many applications without having any concerns over exceeding the range and no compromise in accuracy. The output swings of the EC5579 typically extend to within 80mV of positive and negative supply rails with load currents of 5mA. The output voltage swing can be even closer to the supply rails by merely decreasing the load current. Figure 1 shows the input and output waveforms for the device in the unity-gain configuration. The amplifier is operated under ±5V supply with a 10k load connected to GND. The input is a 10Vp-p sinusoid. An approximately 9.985 Vp-p of output voltage swing can be easily achieved.
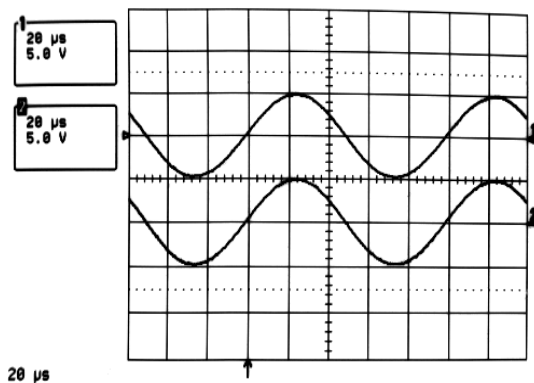


**Figure10. Operation with Rail-to-Rail Input and Output**

### Output Short Circuit Current Limit

A +/-120mA short circuit current will be limited by the EC5579 if the output is directly shorted to the positive or the negative supply. For an indefinitely output short circuit, the power dissipation could easily increase such that the device may be damaged. The internal metal interconnections are well designed to prevent the output continuous current from exceeding +/-30 mA such that the maximum reliability can be well maintained.

## Output Phase Reversal

The EC5579 is designed to prevent its output from being phase reversal as long as the input voltage is limited from $V_{S-}$ 0.5V to $V_{S+}$ 0.5V. Figure 2 shows a photo of the device output with its input voltage driven beyond the supply rails. Although the phase of the device's output will not be reversed, the input's over-voltage should be avoided. An improper input voltage exceeds supply range by more than 0.6V may result in an over stress damage.
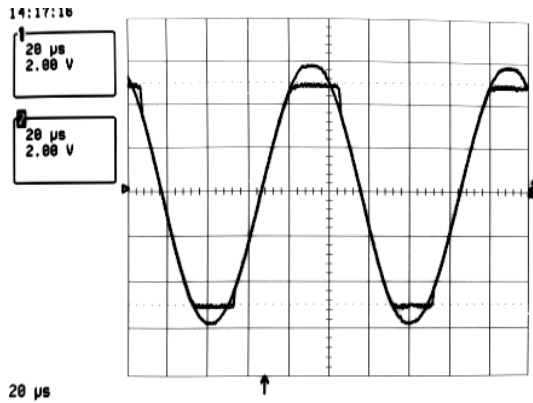


**Figure11. Operation with Beyond-the Rails Input**

### Power Dissipation

The EC5579 is designed for maximum output current capability. Even though momentary output shorted to ground causes little damage to the device.

For the high drive amplifier EC5579, it is possible to exceed the 'absolute-maximum junction temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area. The maximum power dissipation allowed in a package is determined according to:

$$P_{Dmax} = \frac{T_{Jmax} - T_{Amax}}{\Theta_{JA}}$$

Where:

$T_{Jmax}$ = Maximum Junction Temperature

$T_{Amax}$ = Maximum Ambient Temperature

$\Theta_{JA}$ = Thermal Resistance of the Package

$P_{Dmax}$ = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$P_{Dmax} = \sum_i [V_S * I_{Smax} + (V_{S+} - V_O) * I_L]$

When sourcing, and

$P_{Dmax} = \sum_i [V_S * I_{Smax} + (V_O - V_{S-}) * I_L]$

When sinking.

Where:

**i** = 1 to 4

$V_S$ = Total Supply Voltage

$I_{Smax}$ = Maximum Supply Current Per Amplifier

$V_O$ = Maximum Output Voltage of the Application

$I_L$ = Load current

$R_L$ = Load Resistance = $(V_{S+} - V_O)/I_L = (V_O - V_{S-})/ I_L$

A calculation for $R_L$ to prevent device from overheat can be easily solved by setting the two $P_{Dmax}$ equations equal to each other.

| Pin Count | Θja ( /W) | Θjc ( /W) | |
|---|---|---|---|
| TQFP-48 | 35 | 7 | Exposed pad (5.0x5.0 mm) |
| TQFP-48 | 42 | 19.6 | Exposed pad (3.05x3.05 mm) |
| TQFP-48 | 67 | 31 | Normal |

**Driving Capacitive Loads**

The EC5579 is designed to drive a wide range of capacitive loads. In addition, the output current handling capability of the device allows for good slewing characteristics even with large capacitive loads. The combination of these features make the EC5579 ideally for applications such as TFT LCD panel grayscale reference voltage buffers, ADC input amplifiers, etc.

As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking increase. The amplifiers drive 10pF loads in parallel with10K  . with just 1.5dB of peaking, and 100pF with 6.4dB of peaking. If less peaking is desired in these applications, a small series resistor (usually between 5  and 50  ) can be placed in

series with the output. However, this will obviously reduce the gain slightly. Another method of reducing peaking is to add a "snubber" circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150  and 10nF are typical. The advantage of a snubber is that it improves the settling and overshooting performance while does not draw any DC load current or reduce the gain.

**Power Supply Bypassing and Printed Circuit Board Layout**

With high phase margin, the EC5579 performs stable gain at high frequency. Like any high-frequency device, good layout of the printed circuit board usually comes with optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the $V_{S-}$ pin is connected to ground, a 0.1 μF ceramic capacitor should be placed from $V_{S+}$ pin to $V_{S-}$ pin as a bypassing capacitor. A 4.7μF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7μF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.
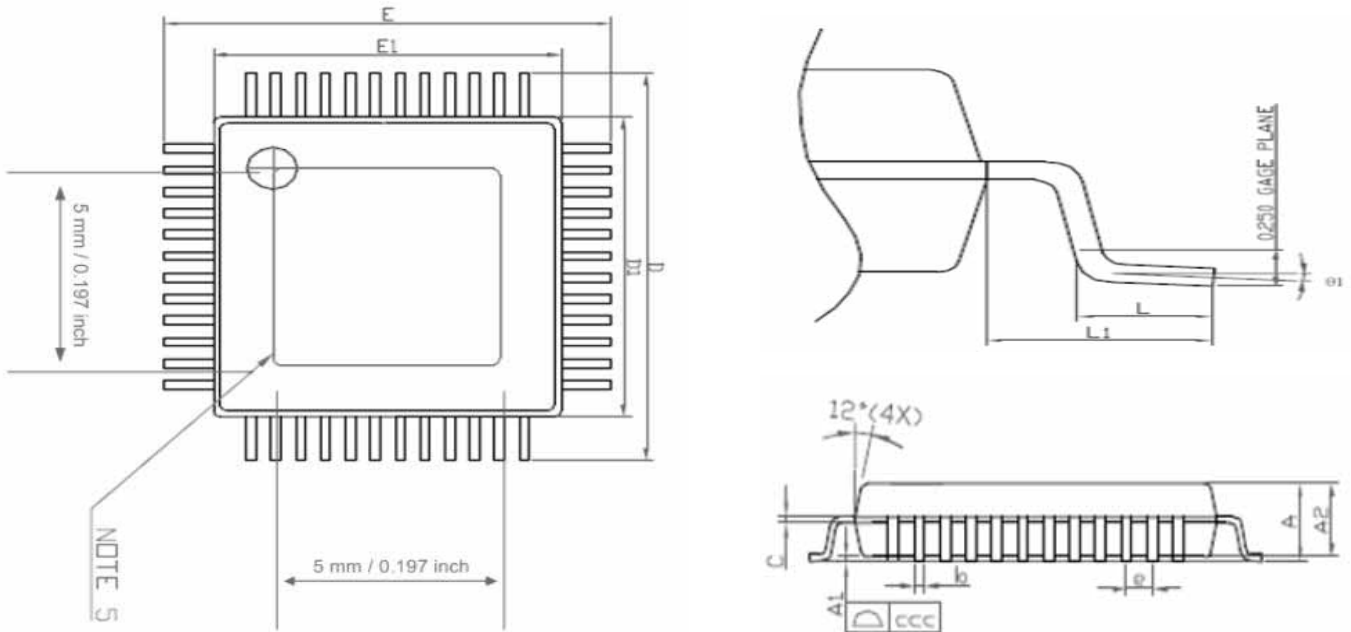
## Application Circuits
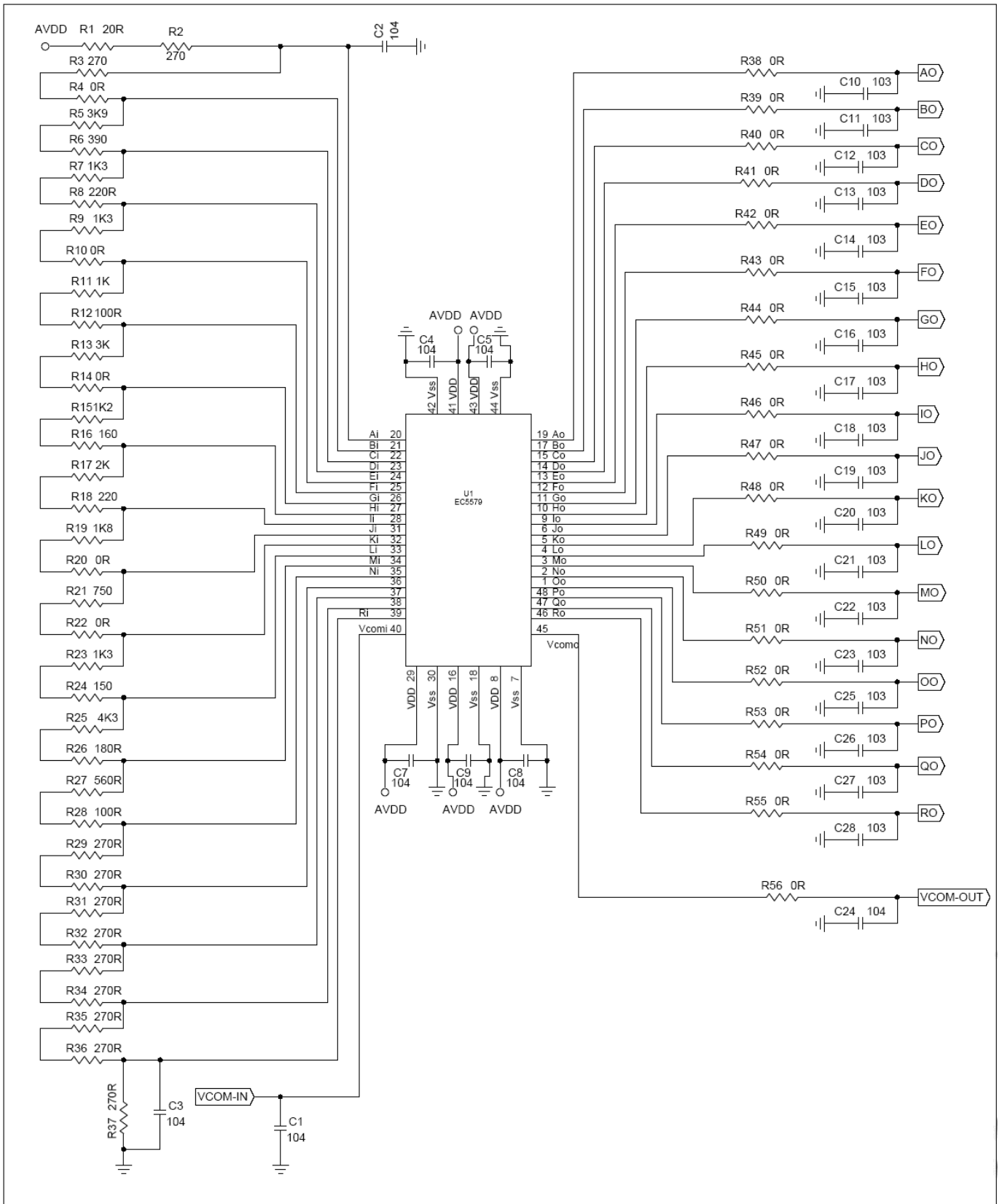
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**OUTLINE DIMENSIONS** (Dimensions shown in millimeters)

H1: **Exposed pad (5.0x5.0 mm)**



| DIMN | Millimeters | | | INCHES | | |
|------|-----|-----|-----|-----|-----|-----|
| | **MIN** | **NOM** | **MAX** | **MIN** | **NOM** | **MAX** |
| A | — | — | 1.15 | — | — | 0.046 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.17 | 0.22 | 0.27 | 0.006 | 0.008 | 0.011 |
| C | 0.09 | — | 0.20 | 0.003 | — | 0.008 |
| D1 | 6.90 | 7.00 | 7.10 | 0.271 | 0.275 | 0.279 |
| D | 8.80 | 9.00 | 9.20 | 0.346 | 0.354 | 0.362 |
| E1 | 6.90 | 7.00 | 7.10 | 0.271 | 0.275 | 0.279 |
| E | 8.80 | 9.00 | 9.20 | 0.346 | 0.354 | 0.362 |
| e | — | 0.5(TYP) | — | — | 0.02(TYP) | — |
| L | 0.45 | 0.6 | 0.75 | 0.018 | 0.024 | 0.029 |
| L1 | — | 1.00(REF) | — | — | 0.039(REF) | — |
| Q1 | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | — | — | 0.08 | — | — | 0.003 |

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLE FLASH AND GATE BURRS.
2. DIMENSION L IS MEASURED IN GAGE PLANE.
3. TOLERANCE 0.10mm UNLESS OTHERWISE SPECIFIED.
4. CONTROLLING DIMENSION IS MILLIMETER CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. DIE PA D EXPOSURE SIZE IS ACCORING TO LEAD FRAME DESIGN.
6. FOLLOWED FORM JEDEC MO-136.

## OUTLINE DIMENSIONS (Dimensions shown in millimeters)
### H: Exposed pad (3.05x3.05 mm)



(THERMALLY ENHANCED VARIATIONS ONLY)
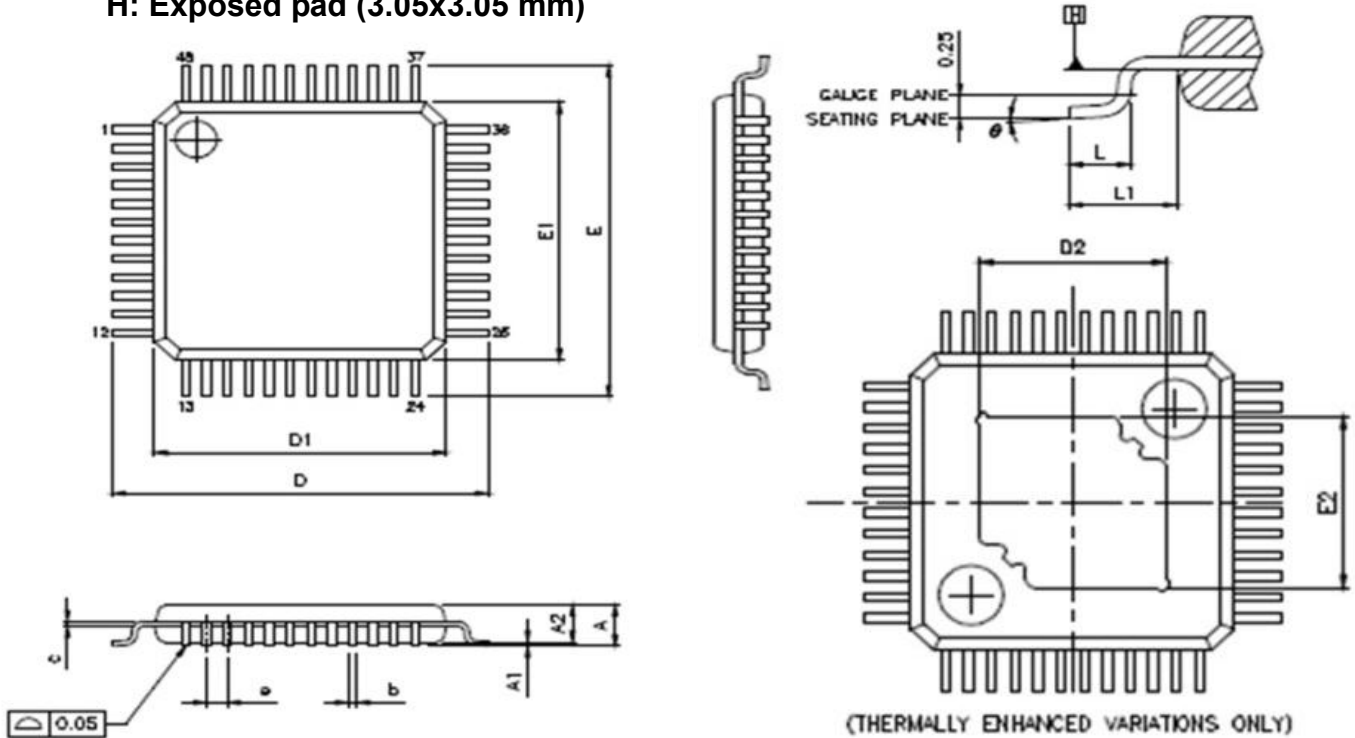
THERNALLY ENHANCED DINENSIONS (SHOW IN WW)

| PAD SIZE | E2 | | D2 | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| 160X16E | 3.05 | 4.06 | 3.05 | 4.06 |

| DIMN | MM | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b | 0.17 | 0.20 | 0.23 |
| c | 0.09 | — | 0.16 |
| D | 9.00 BSC | | |
| D1 | 7.00 BSC | | |
| E | 9.00 BSC | | |
| E1 | 7.00 BSC | | |
| e | 0.50 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00(REF) | | |
| Q | 0˚ | 3.5˚ | 7˚ |

NOTE

1. JEDEC OUTLINE:

   NS-026 ABC

   NS-026 ABC-HD (THERNALLY ENHANCED VARIATIONS ONLY)

2. DATUN PLANE H IS LOCATED AT THE BOTTOM OF THE MOLE PATTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3. DIMENSIONS D1 AND E1 DO NOR INCLUDE MOLD PROTRUSION.ALLOWABLE PROTRUSION IS 0.25mm PER SIDE.DIMENSICNS D1 AND E1 DO INCLUDE MOLD MISWATCH AND ARE DETERMINED AT DATUN PLANE H

4.DINENSION b DOES NOT INCLUDE DANBAR PROTRUSION.