TOP209/210

TOPSwitch® Family

Three-terminal Off-line PWM Switch

Product Highlights

Cost Effective Switcher for Low Power Applications

- Replaces linear power supplies
- Replaces discrete switcher and 20 to 50 components – cuts cost, increases reliability
- Stand-by power supplies for Green or energy efficient products such as personal computers, monitors, UPS, copiers, fax machines, etc.
- Housekeeping or "keep-alive" power supply applications such as TV, appliances, industrial control and personal computers
- Meets 'Blue Angel' low power stand-by specification
- Controlled MOSFET turn-on reduces EMI and EMI filter costs
- 80% smaller and lighter compared to linear supply
- 50% smaller compared to discrete switcher

Over 80% Efficiency in Flyback Topology

- Built-in start-up and current limit reduce DC losses
- Low capacitance 700 V MOSFET cuts AC losses
- CMOS controller/gate driver consumes only 6 mW
- 70% maximum duty cycle minimizes conduction losses

Simplifies Design – Reduces Time to Market

- Supported by reference design boards
- Integrated PWM Controller and 700 V MOSFET in industry standard eight pin DIP package
- Only one external capacitor needed for compensation, bypass and start-up/auto-restart functions
- Easily interfaces with both opto and primary feedback

System Level Fault Protection Features

- Auto-restart and cycle by cycle current limiting functions handle both primary and secondary faults
- On-chip thermal shutdown with hysteresis protects the entire system against overload

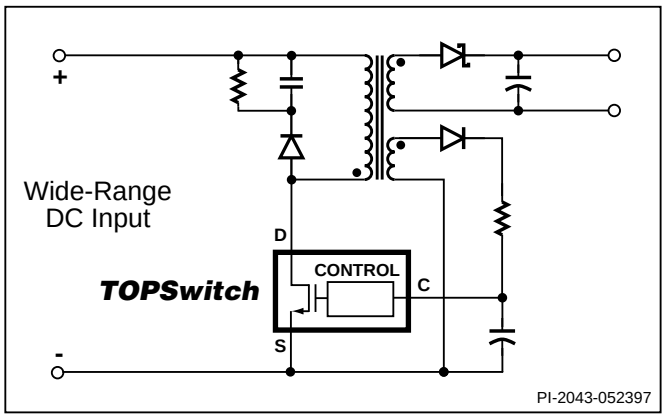


Figure 1. Typical Application.

TOPSwitch **Selection Guide**

ORDER PART NUMBER	PACKAGE	OUTPUT POWER RANGE	
		230 VAC or 110 VAC w/Doubler	85-265 VAC
TOP209P	DIP-8	0-4 W	0-2 W
TOP209G	SMD-8		
TOP210PFI	DIP-8	0-8 W	0-5 W
TOP210G	SMD-8		

Description

The TOP209/210 implements all functions necessary for an off-line switched mode control system: high voltage N-channel power MOSFET with controlled turn-on gate driver, voltage mode PWM controller with integrated oscillator, high voltage start-up bias circuit, bandgap derived reference, bias shunt regulator/error amplifier for loop compensation and fault protection circuitry. Compared to discrete MOSFET and controller or self oscillating (RCC) switching converter solutions, a *TOPSwitch* integrated circuit can reduce total cost, component count, size, weight and at the same time increase efficiency and system reliability. The TOP209/210 are intended for 100/110/230 VAC off-line Power Supply applications in the 0 to 8 W (0 to 5 W universal) range.

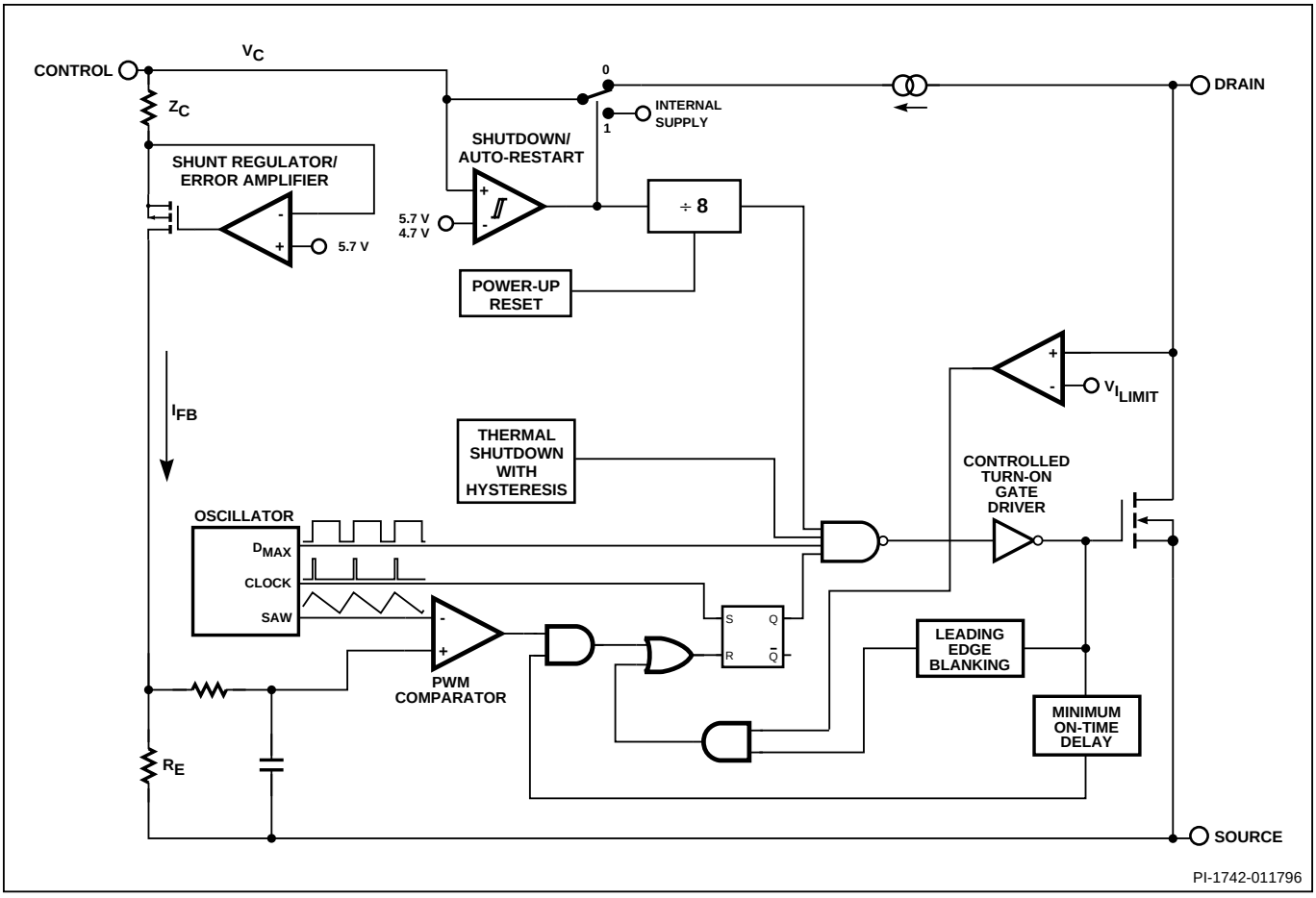


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN Pin:
Output MOSFET drain connection. Provides internal bias current during start-up operation via an internal switched high-voltage current source. Internal current sense point.

CONTROL Pin:
Error amplifier and feedback current input pin for duty cycle control. Internal shunt regulator connection to provide internal bias current during normal operation. It is also used as the supply bypass and auto-restart/compensation capacitor connection point.

SOURCE Pin:
Control circuit common, internally connected to output MOSFET source.

SOURCE (HV RTN) Pin:
Output MOSFET source connection for high voltage return.

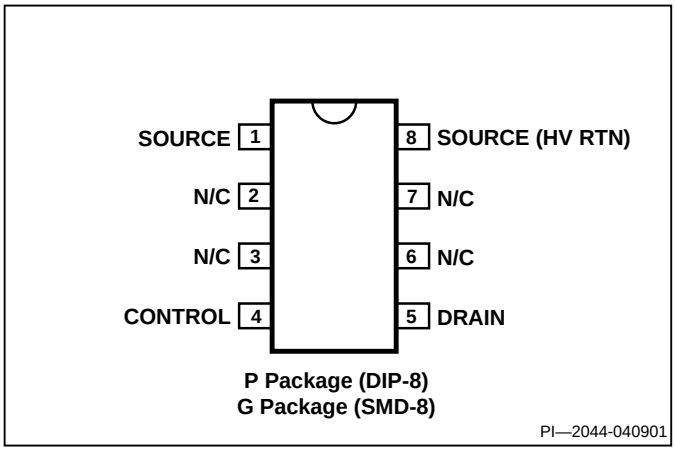


Figure 3. Pin Configuration.

TOPSwitch Family Functional Description

TOPSwitch is a self biased and protected linear control current-to-duty cycle converter with an open drain output. High efficiency is achieved through the use of CMOS and integration of the maximum number of functions possible. CMOS significantly reduces bias currents as compared to bipolar or discrete solutions. Integration eliminates external power resistors used for current sensing and/or supplying initial start-up bias current.

During normal operation, the internal output MOSFET duty cycle linearly decreases with increasing CONTROL pin current as shown in Figure 4. To implement all the required control, bias, and protection functions, the DRAIN and CONTROL pins each perform several functions as described below. Refer to Figure 2 for a block diagram and Figure 6 for timing and voltage waveforms of the *TOPSwitch* integrated circuit.

Control Voltage Supply

CONTROL pin voltage V_C is the supply or bias voltage for the controller and driver circuitry. An external bypass capacitor closely connected between the CONTROL and SOURCE pins is required to supply the gate drive current. The total amount of capacitance connected to this pin (C_T) also sets the auto-restart timing as well as control loop compensation. V_C is regulated in either of two modes of operation. Hysteretic regulation is used for initial start-up and overload operation. Shunt regulation is used to separate the duty cycle error signal from the control circuit supply current. During start-up, V_C current is supplied from a high-voltage switched current source connected internally between the DRAIN and CONTROL pins. The current source provides sufficient current to supply the control circuitry as well as charge the total external capacitance (C_T).

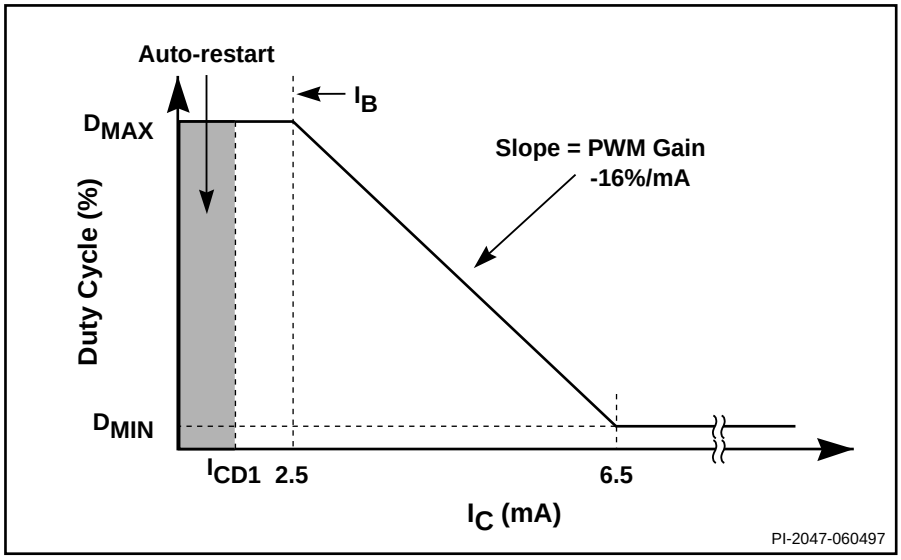


Figure 4. Relationship of Duty Cycle to CONTROL Pin Current.

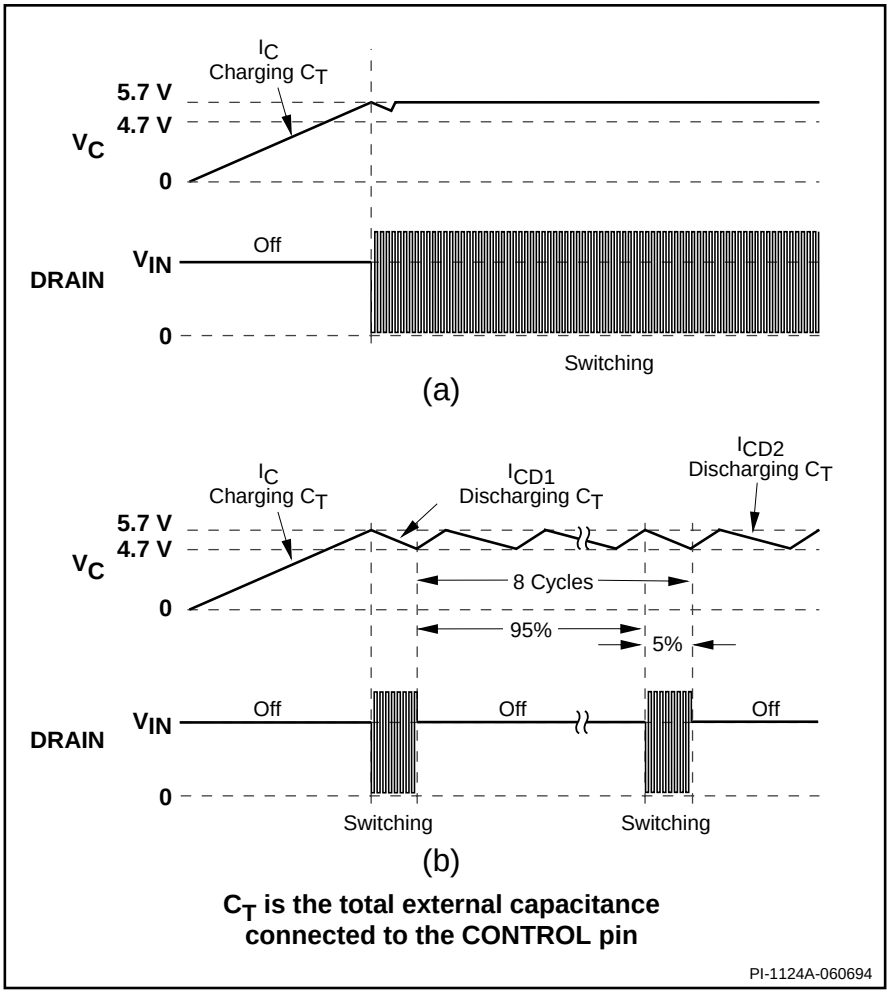


Figure 5. Start-up Waveforms for (a) Normal Operation and (b) Auto-restart.

TOPSwitch Family Functional Description (cont.)

The first time V_C reaches the upper threshold, the high-voltage current source is turned off and the PWM modulator and output transistor are activated, as shown in Figure 5(a). During normal operation (when the output voltage is regulated) feedback control current supplies the V_C supply current. The shunt regulator keeps V_C at typically 5.7 V by shunting CONTROL pin feedback current exceeding the required DC supply current through the PWM error signal sense resistor R_E. The low dynamic impedance of this pin (Z_C) sets the gain of the error amplifier when used in a primary feedback configuration. The dynamic impedance of the CONTROL pin together with the external resistance and capacitance determines the control loop compensation of the power system.

If the CONTROL pin external capacitance (C_T) should discharge to the lower threshold, then the output MOSFET is turned off and the control circuit is placed in a low-current standby mode. The high-voltage current source is turned on and charges the external capacitance again. Charging current is shown with a negative polarity and discharging current is shown with a positive polarity in Figure 6. The hysteretic auto-restart comparator keeps V_C within a window of typically 4.7 to 5.7 V by turning the high-voltage current source on and off as shown in Figure 5(b). The auto-restart circuit has a divide-by-8 counter which prevents the output MOSFET from turning on again until eight discharge-charge cycles have elapsed. The counter effectively limits *TOPSwitch* power dissipation by reducing the auto-restart duty cycle to typically 5%. Auto-restart continues to cycle until output voltage regulation is again achieved.

Bandgap Reference

All critical *TOPSwitch* internal voltages are derived from a temperature-compensated bandgap reference. This reference is also used to generate a temperature-compensated current source which is trimmed to accurately set the oscillator frequency and MOSFET gate drive current.

Oscillator

The internal oscillator linearly charges and discharges the internal capacitance between two voltage levels to create a sawtooth waveform for the pulse width modulator. The oscillator sets the pulse width modulator/current limit latch at the beginning of each cycle. The nominal frequency of 100 kHz was chosen to minimize EMI and maximize efficiency in power supply applications. Trimming of the current reference improves oscillator frequency accuracy.

Pulse Width Modulator

The pulse width modulator implements a voltage-mode control loop by driving the output MOSFET with a duty cycle inversely proportional to the current flowing into the CONTROL pin. The error signal across R_E is filtered by an RC network with a typical corner frequency of 7 kHz to reduce the effect of switching noise. The filtered error signal is compared with the internal oscillator sawtooth waveform to generate the duty cycle waveform. As the control current increases, the duty cycle decreases. A clock signal from the oscillator sets a latch which turns on the output MOSFET. The pulse width modulator resets the latch, turning off the output MOSFET. The maximum duty cycle is set by the symmetry of the internal oscillator. The modulator has a minimum ON-time to keep the current consumption of the *TOPSwitch* independent of the error signal. Note that a minimum current must be driven into the CONTROL pin before the duty cycle begins to change.

Gate Driver

The gate driver is designed to turn the output MOSFET on at a controlled rate to minimize common-mode EMI. The gate drive current is trimmed for improved accuracy.

Error Amplifier

The shunt regulator can also perform the function of an error amplifier in primary feedback applications. The shunt regulator voltage is accurately derived from the temperature compensated bandgap reference. The gain of the error amplifier is set by the CONTROL pin dynamic impedance. The CONTROL pin clamps external circuit signals to the V_C voltage level. The CONTROL pin current in excess of the supply current is separated by the shunt regulator and flows through R_E as the error signal.

Cycle-By-Cycle Current Limit

The cycle by cycle peak drain current limit circuit uses the output MOSFET ON-resistance as a sense resistor. A current limit comparator compares the output MOSFET ON-state drain-source voltage, $V_{DS(ON)}$, with a threshold voltage. High drain current causes $V_{DS(ON)}$ to exceed the threshold voltage and turns the output MOSFET off until the start of the next clock cycle. The current limit comparator threshold voltage is temperature compensated to minimize variation of the effective peak current limit due to temperature related changes in output MOSFET $R_{DS(ON)}$.

The leading edge blanking circuit inhibits the current limit comparator for a short time after the output MOSFET is turned on. The leading edge blanking time has been set so that current spikes caused by primary-side capacitances and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse.

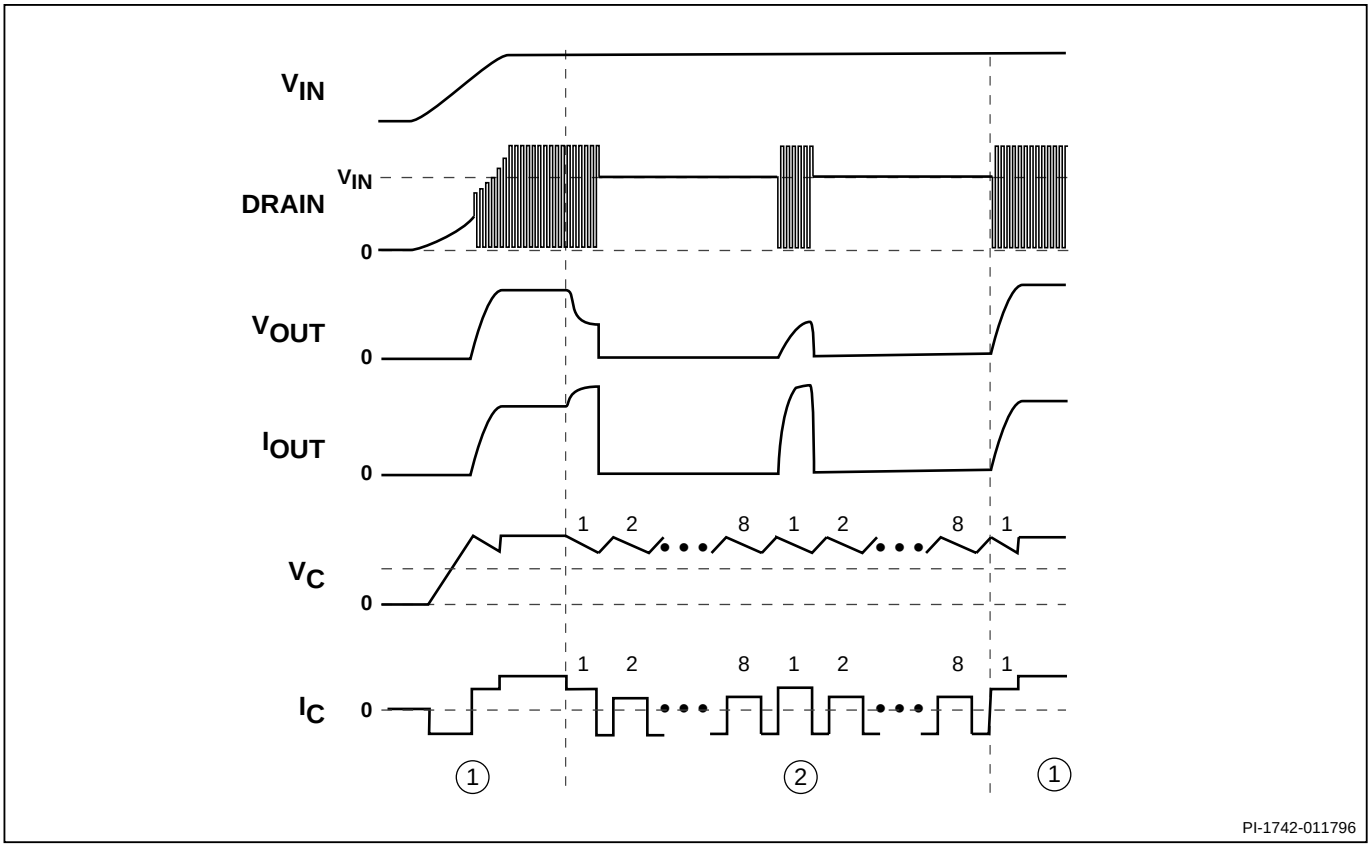


Figure 6. Typical Waveforms for (1) Normal Operation, (2) Auto-restart.

Shutdown/Auto-restart

To minimize *TOPSwitch* power dissipation, the shutdown/ auto-restart circuit turns the power supply on and off at a duty cycle of typically 5% if an out of regulation condition persists. Loss of regulation interrupts the external current into the CONTROL pin. V_C regulation changes from shunt mode to the hysteretic auto-restart mode described above. When the fault condition is removed, the power supply output becomes regulated, V_C regulation returns to shunt mode, and normal operation of the power supply resumes.

Hysteretic Overtemperature Protection

Temperature protection is provided by a precision analog circuit that turns the output MOSFET off when the junction temperature exceeds the thermal shutdown temperature (typically 145 °C). When the junction temperature cools past the hysteresis temperature, normal operation resumes. V_C is regulated in hysteretic mode while the power supply is turned off.

High-voltage Bias Current Source

This current source biases *TOPSwitch* from the DRAIN pin and charges the CONTROL pin external capacitance (C_T) during start-up or hysteretic operation. The current source is switched on and off with an effective duty cycle of approximately 35%. This duty cycle is determined by the ratio of CONTROL pin charge (I_C) and discharge currents (I_{CD1} and I_{CD2}). This current source is turned off during normal operation when the output MOSFET is switching.

General Circuit Description

Figure 7 shows a low-cost, DC input, flyback switching power supply using the TOP210 integrated circuit. This 5 V, 4 W power supply operates from a DC voltage derived from rectified and filtered AC mains voltage of 85 to 265 VAC. The 5 V output is indirectly sensed via the primary bias winding. The output voltage is determined by the *TOPSwitch* CONTROL pin shunt regulator voltage (V_C), the voltage drops of rectifiers D2 and D3, and the turns ratio between the bias winding and output winding of T1. Other output voltages are also possible by adjusting the transformer turns ratios.

The high voltage DC bus is applied to the primary winding of T1. Capacitor C1 filters the high voltage supply, and is only necessary if the connections between the high voltage DC supply and the TOP210 are long. The other side of the transformer primary is driven by the integrated high-voltage MOSFET within the TOP210. D1 and VR1 clamp the voltage spike caused by transformer leakage inductance to a safe value and reduce ringing at the DRAIN of U1. The power secondary winding is rectified and filtered by D2, C2, L1, and C3 to create the 5V output voltage. The bias winding is rectified and filtered by D3, R1 and C5 to create a bias voltage to the TOP210. C5 also filters internal MOSFET gate drive charge current spikes on the CONTROL pin, determines the auto-restart frequency, and together with R1, compensates the control loop.

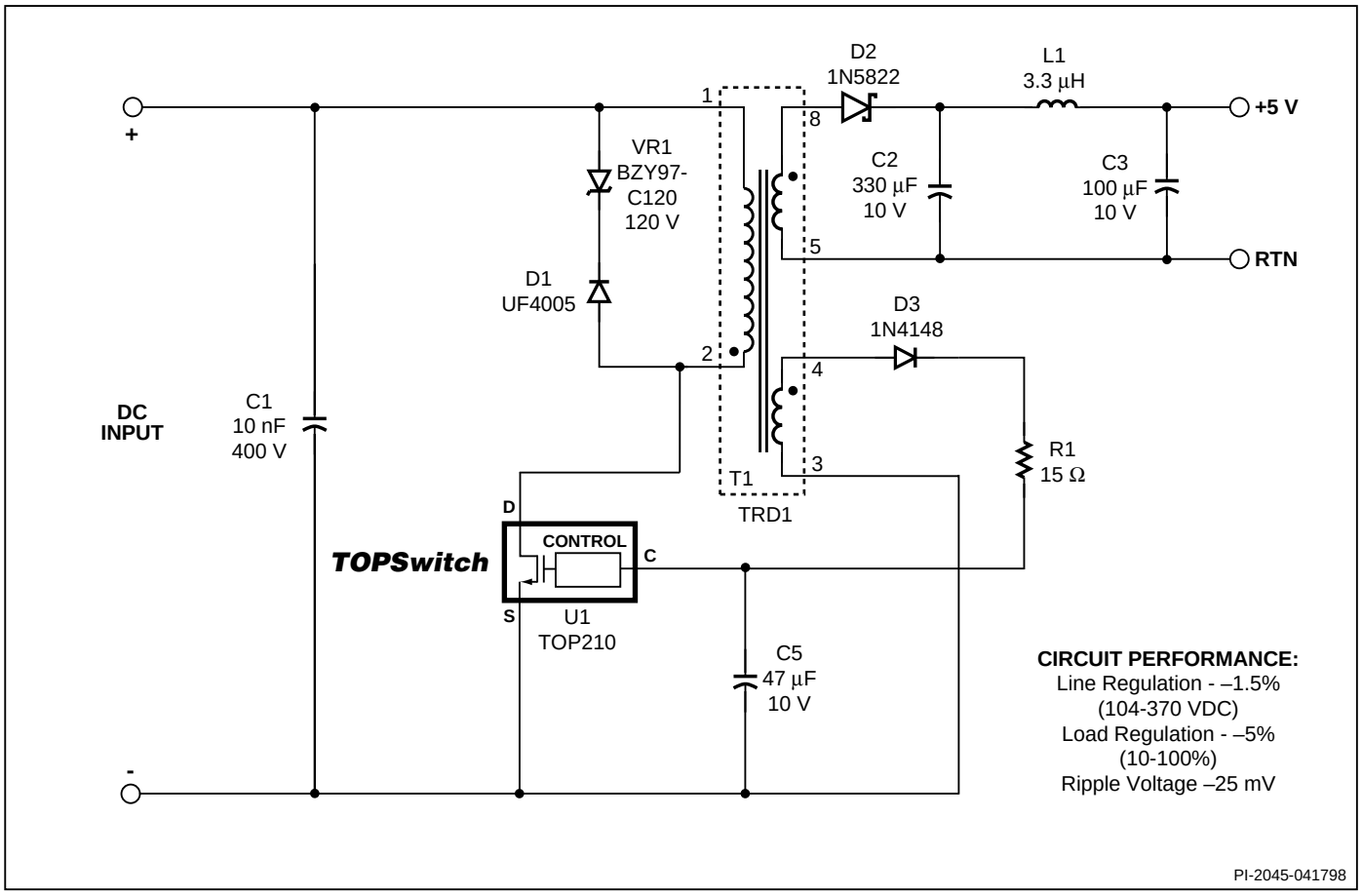


Figure 7. Schematic Diagram of a Minimum Parts Count 5 V, 4 W Bias Supply Using the TOP210.

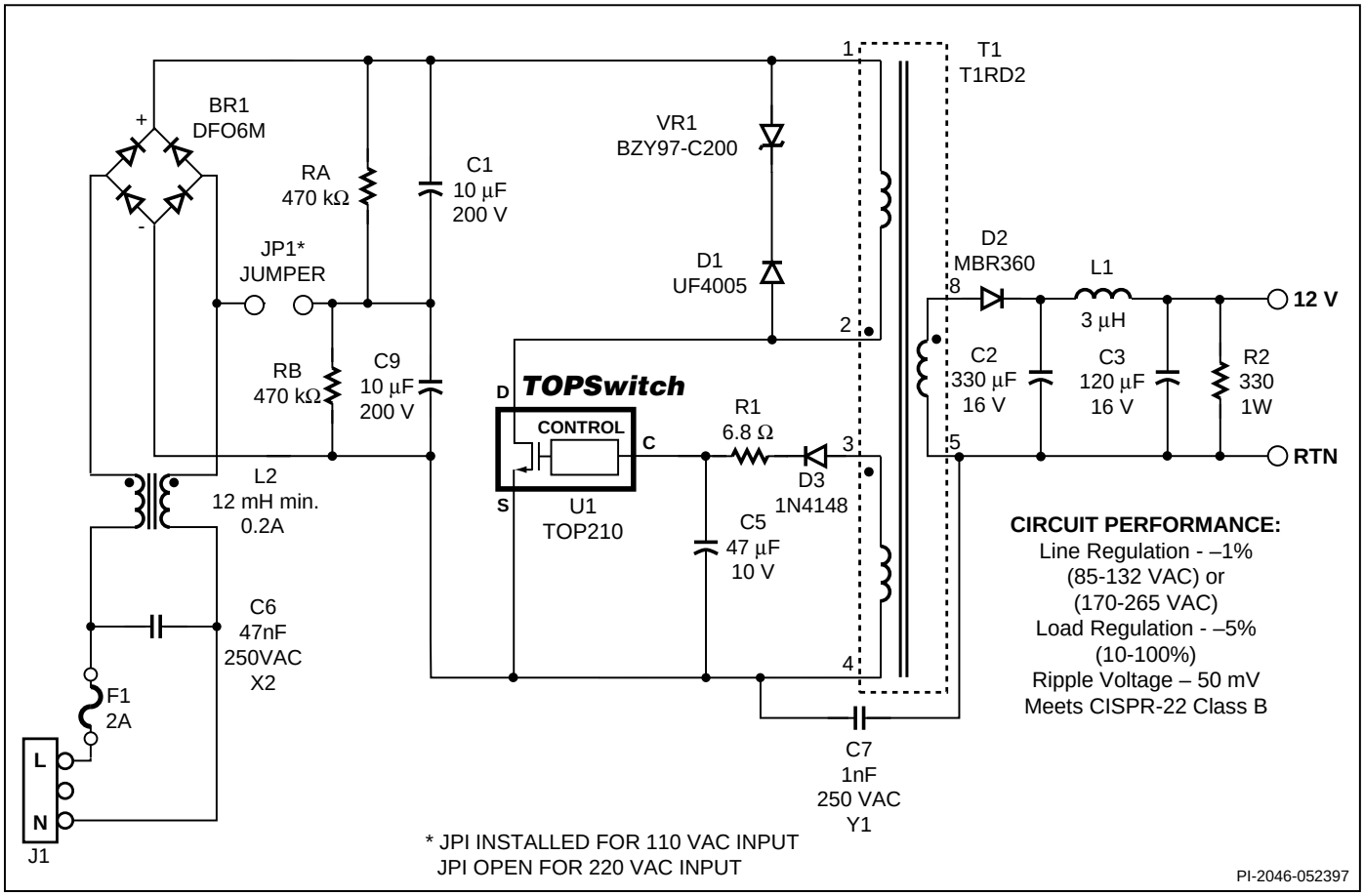


Figure 8. Schematic Diagram of a 12 V, 8 W 110/220 VAC Input Power Supply Using the TOP210.

The circuit shown in Figure 8 produces a 12 V, 8 W power supply that operates from 85 to 132 VAC or 170 to 264 VAC input voltage. The 12 V output voltage is determined by the *TOPSwitch* CONTROL pin shunt regulator voltage, the voltage drops of D2 and D3, and the turns ratio between the bias and output windings of T1. Other output voltages are also possible by adjusting the transformer turns ratios. R1 and C5 provide filtering of the bias winding to improve line and load regulation.

AC power is rectified and filtered by BR1, C1 and C9 to create the high voltage DC bus applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated high-voltage MOSFET within the TOP210. JP1 is a jumper used to select 110 VAC or 220 VAC operation. Installing JP1 selects 110 VAC operation. Leaving JP1 open selects 220 VAC operation. RA and RB, which equalize voltage across C1 and C9, are necessary only when JP1 is not installed. D1 and VR1 clamp the leading-edge voltage spike caused by transformer leakage inductance to a safe value and reduce ringing. The power secondary winding is rectified and filtered by D2, C2, L1, and C3 to create the 12 V output voltage. R2 provides a pre-load on the 12 V output to improve load regulation at light loads. The bias winding is rectified and filtered by D3, R1, and C5 to create a bias voltage to the TOP210. L2 and Y1-capacitor C7 attenuate common-mode emission currents caused by high-voltage switching waveforms on the DRAIN side of the primary winding and the primary to secondary capacitance. L2 and C6 attenuate differential-mode emission currents caused by the fundamental and harmonics of the trapezoidal primary current waveform. C5 filters internal MOSFET gate drive charge current spikes on the CONTROL pin, determines the auto-restart frequency, and together with R1, compensates the control loop.

Key Application Considerations

Use a Kelvin connection to the SOURCE pin for the CONTROL pin bypass capacitor as shown in Figure 9.

Minimize peak voltage and ringing on the DRAIN voltage at turn-off. Use a Zener or TVS Zener diode to clamp the DRAIN voltage.

Under some conditions, externally provided bias or supply current driven into the CONTROL pin can hold the *TOPSwitch* in one of the 8 auto-restart cycles indefinitely and prevent starting. Shorting the CONTROL pin to the SOURCE pin will reset the *TOPSwitch*. To avoid this problem when doing bench evaluations, it is recommended that the V_C power supply be turned on before the DRAIN voltage is applied.

CONTROL pin currents during auto-restart operation are much lower at low input voltages (< 20 V) which increases the auto-restart cycle period (see the I_C vs. Drain Voltage Characteristic curve).

Short interruptions of AC power may cause *TOPSwitch* to enter the 8-count auto-restart cycle before starting again. This is because the input energy storage capacitors are not completely discharged and the CONTROL pin capacitance has not discharged below the internal power-up reset voltage ($V_{C(RESET)}$).

In some cases, minimum loading may be necessary to keep a lightly loaded or unloaded output voltage within the desired range due to the minimum ON-time.

For additional applications information regarding the *TOPSwitch* family, refer to AN-14 in the 1996-97 Data Book and Design Guide or on our Web site.

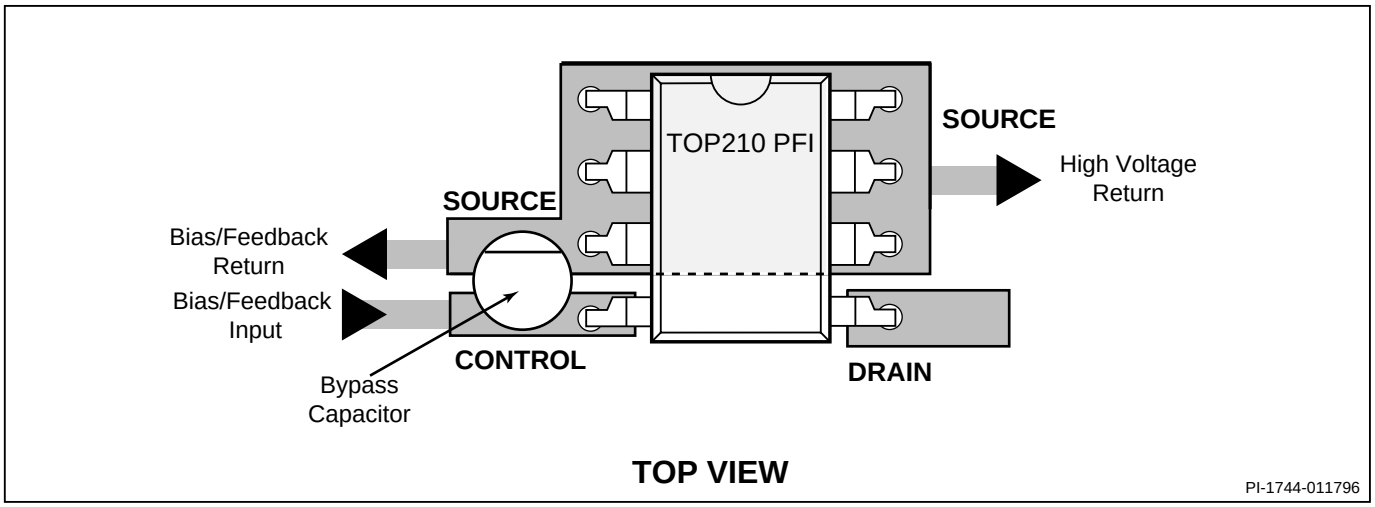


Figure 9. Recommended PC Layout for the TOP209/210.

ABSOLUTE MAXIMUM RATINGS(1)

DRAIN Voltage ..... - 0.3 to 700 V
CONTROL Voltage ..... - 0.3 V to 9 V
CONTROL Current ..... 100 mA

Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature(2) ..... -40 to 150 °C
Lead Temperature(3) ..... 260 °C
Thermal Impedance (θ_{JA}) ..... 100 °C/W
Thermal Impedance (θ_{JC}) ..... 40 °C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.

Parameter	Symbol	Conditions (Unless Otherwise Specified) See Figure 12 SOURCE = 0 V T_J = -40 to 125 °C		Min	Typ	Max	Units
CONTROL FUNCTIONS							
Output Frequency	f_{OSC}	I_C = 4 mA, T_J = 25 °C	TOP209	55	70	85	kHz
			TOP210	90	100	110	
Maximum Duty Cycle	D_{MAX}	$I_C = I_{CD1}$ + 0.5 mA, See Figure 10		64	67	70	%
Minimum Duty Cycle	D_{MIN}	I_C = 10 mA See Figure 10	TOP209	0.5	1.5	2.5	%
			TOP210	1.0	1.8	3.0	
PWM Gain		I_C = 4 mA, T_J = 25 °C See Figure 4		-11	-16	-21	%/mA
PWM Gain Temperature Drift		See Note A			-0.05		%/mA/°C
External Bias Current	I_B	See Figure 4		1.5	2.5	4	mA
Dynamic Impedance	Z_C	I_C = 4 mA, T_J = 25 °C See Figure 11		10	15	22	Ω
Dynamic Impedance Temperature Drift					0.18		%/°C
SHUTDOWN/AUTO-RESTART							
CONTROL Pin Charging Current	I_C	T_J = 25 °C	V_C = 0 V	-2.4	-1.9	-1.2	mA
			V_C = 5 V	-2	-1.5	-0.8	
Charging Current Temperature Drift		See Note A			0.4		%/°C
Auto-restart Threshold Voltage	$V_{C(AR)}$	S1 open			5.7		V

Parameter	Symbol	Conditions (Unless Otherwise Specified) See Figure 12 SOURCE = 0 V T_J = -40 to 125 °C		Min	Typ	Max	Units
SHUTDOWN/AUTO-RESTART (cont.)							
UV Lockout Threshold Voltage		S1 open		4.4	4.7	5.0	V
Auto-restart Hysteresis Voltage		S1 open		0.6	1.0		V
Auto-restart Duty Cycle		S1 open			5	9	%
Auto-restart Frequency		S1 open			1.2		Hz
CIRCUIT PROTECTION							
Self-protection Current Limit	I_{LIMIT}	di/dt = 40 mA/µs, T_J = 25 °C	TOP209	0.150		0.230	A
			TOP210	0.230		0.300	
Leading Edge Blanking Time	t_{LEB}	I_C = 4 mA			150		ns
Current Limit Delay	t_{ILD}	I_C = 4 mA			100		ns
Thermal Shutdown Temperature		I_C = 4 mA		125	145		°C
Thermal Shutdown Hysteresis					30		°C
Power-up Reset Threshold Voltage	$V_{C(RESET)}$	S2 open		2.0	3.3	4.2	V

Parameter	Symbol	Conditions (Unless Otherwise Specified) See Figure 12 SOURCE = 0 V T_J = -40 to 125 °C		Min	Typ	Max	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 25 mA	T_J = 25 °C		31.2	36.0	Ω
			T_J = 100 °C		51.4	59.4	
OFF-State Current	I_{DSS}	See Note B V_{DS} = 560 V, T_A = 125 °C				250	µA
Breakdown Voltage	BV_{DSS}	See Note B, I_D = 100 µA, T_A = 25 °C		700			V
Rise Time	t_R	Measured in a Typical Flyback Converter Application			100		ns
Fall Time	t_F				50		ns
DRAIN Supply Voltage		See Note C		36			V
SUPPLY							
Shunt Regulator Voltage	$V_{C(SHUNT)}$	I_C = 4 mA		5.5	5.8	6.1	V
Shunt Regulator Temperature Drift					±50		ppm/°C
CONTROL Supply/ Discharge Current	I_{CD1}	Output MOSFET Enabled		0.6	1.2	1.6	mA
	I_{CD2}	Output MOSFET Disabled		0.5	0.8	1.1	

NOTES:

A. For specifications with negative values, a negative temperature coefficient corresponds to an increase in magnitude with increasing temperature, and a positive temperature coefficient corresponds to a decrease in magnitude with increasing temperature.

B. The breakdown & leakage measurements can be accomplished by using the *TOPSwitch* auto-restart feature. The divide-by-8 counter in the auto-restart circuitry disables the output MOSFET from switching in 7 out of 8 cycles. To place the *TOPSwitch* in one of these cycles, the following procedure can be carried out using the modified circuit of Figure 12:

NOTES: (continued)

i. The 470 Ω 5 W load resistor at the DRAIN pin should be shorted. S1 & S2 should stay closed.
ii. The 40 V output supply should be replaced with a curve tracer capable of forcing 700 V.
iii. The curve tracer should initially be set at 0 V. The 0-50 V variable supply should be adjusted through a voltage sequence of 0 V, 6.5 V, 4.2 V, and 6.5 V.
iv. The breakdown and the leakage measurements can now be taken with the curve tracer. The maximum voltage from the curve tracer must be limited to 700 V under all conditions.

C. It is possible to start up and operate *TOPSwitch* at DRAIN voltages well below 36 V. However, the CONTROL pin charging current is reduced, which affects start-up time and auto-restart frequency and duty cycle. Refer to the characteristic graph on CONTROL pin charge current (I_C) vs. DRAIN voltage for low voltage operation characteristics.

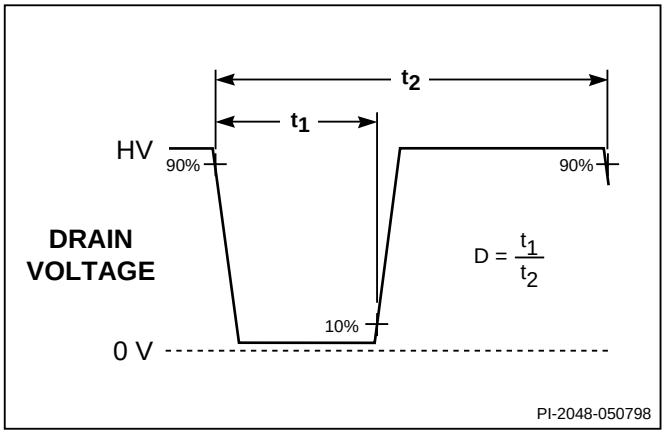


Figure 10. TOPSwitch Duty Cycle Measurement.

TYPICAL CONTROL PIN I-V CHARACTERISTIC

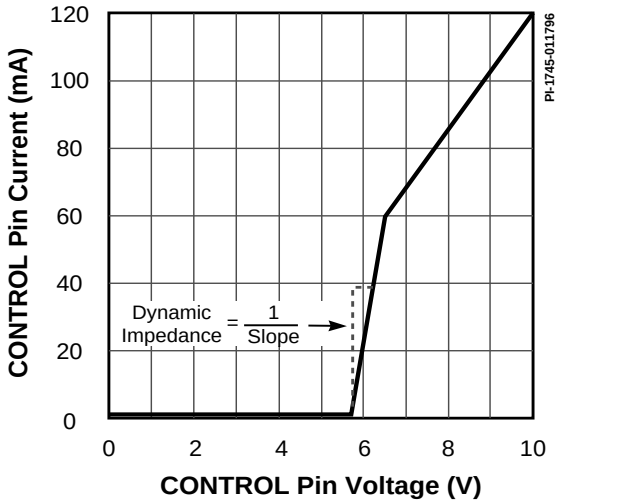


Figure 11. TOPSwitch CONTROL Pin I-V Characteristic.

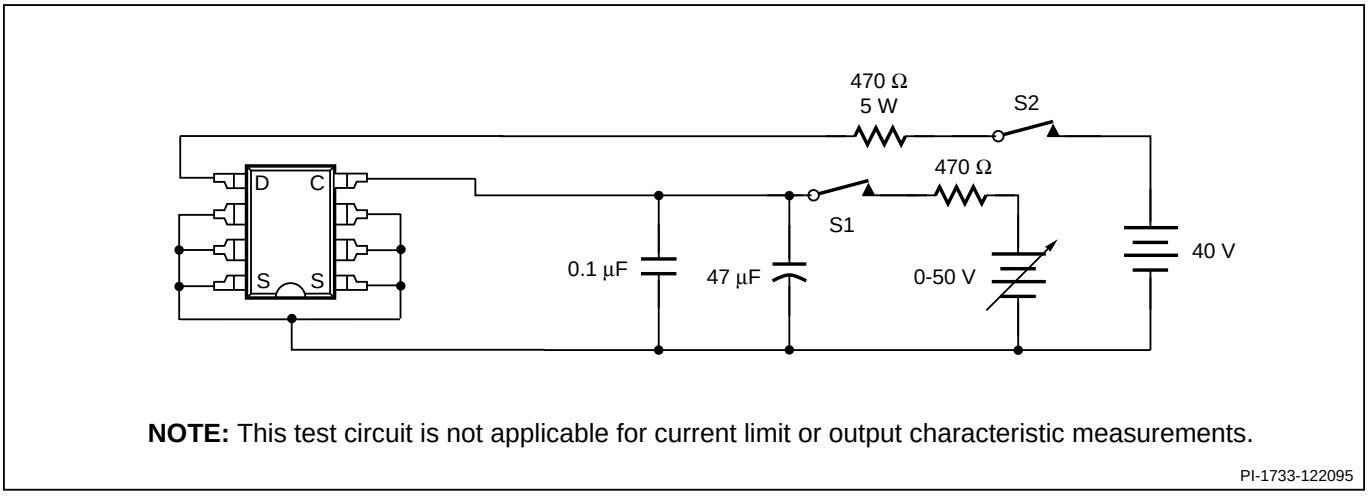


Figure 12. TOPSwitch General Test Circuit.

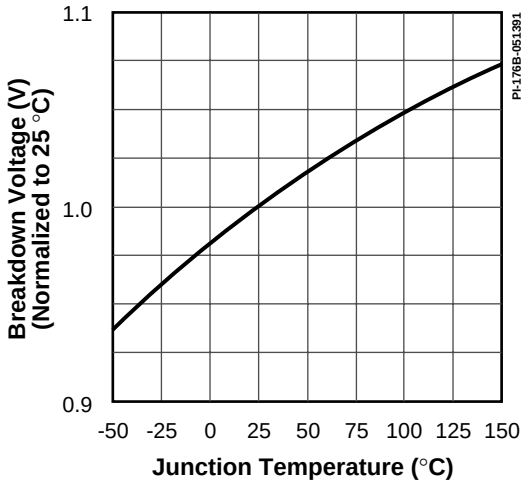
BENCH TEST PRECAUTIONS FOR EVALUATION OF ELECTRICAL CHARACTERISTICS

The following precautions should be followed when testing *TOPSwitch* by itself outside a power supply. The schematic shown in Figure 12 is suggested for laboratory testing of *TOPSwitch*.

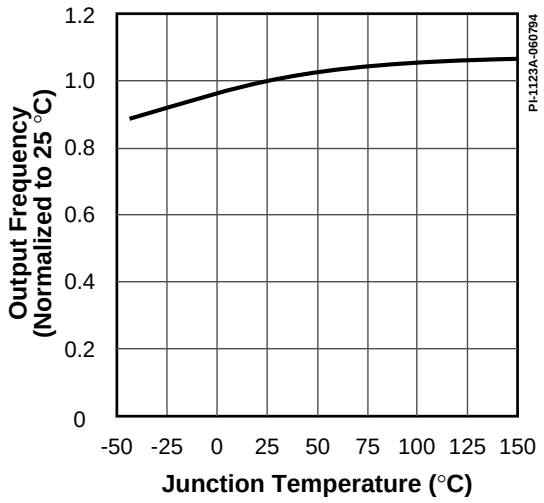
When the DRAIN supply is turned on, the part will be in the auto-restart mode. The CONTROL pin voltage will be oscillating at a low frequency from 4.7 to 5.7 V and the DRAIN is turned on every eighth cycle of the CONTROL pin oscillation. If the CONTROL pin power supply is turned on while in this auto-restart mode, there is only a 12.5% chance that the CONTROL pin oscillation will be in the correct state (DRAIN active state) so that the continuous DRAIN voltage waveform may be observed. It is recommended that the V_C power supply be turned on first and the DRAIN power supply second if continuous DRAIN voltage waveforms are to be observed. The 12.5% chance of being in the correct state is due to the 8:1 counter.

Typical Performance Characteristics

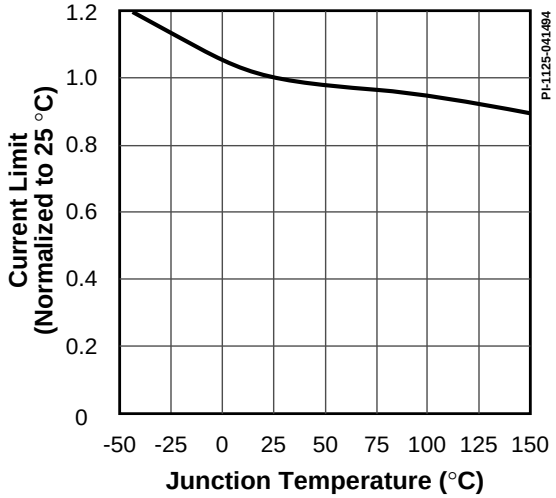
BREAKDOWN vs. TEMPERATURE



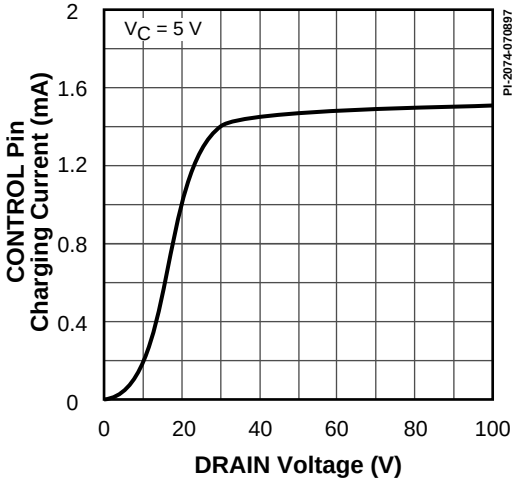
FREQUENCY vs. TEMPERATURE



CURRENT LIMIT vs. TEMPERATURE

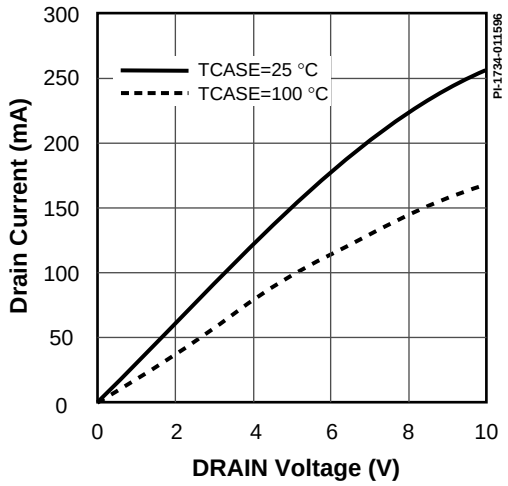


I_C vs. DRAIN VOLTAGE

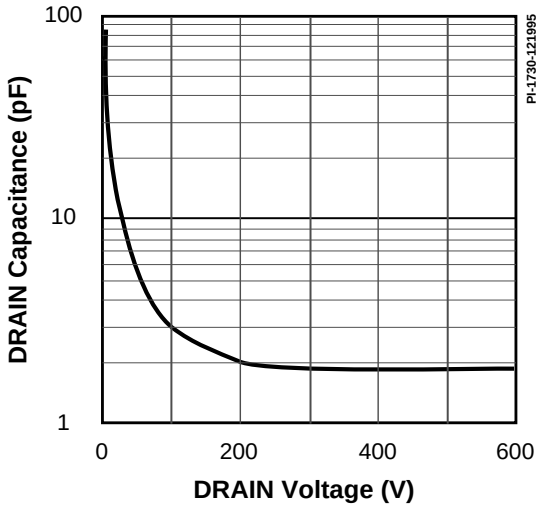


Typical Performance Characteristics (cont.)

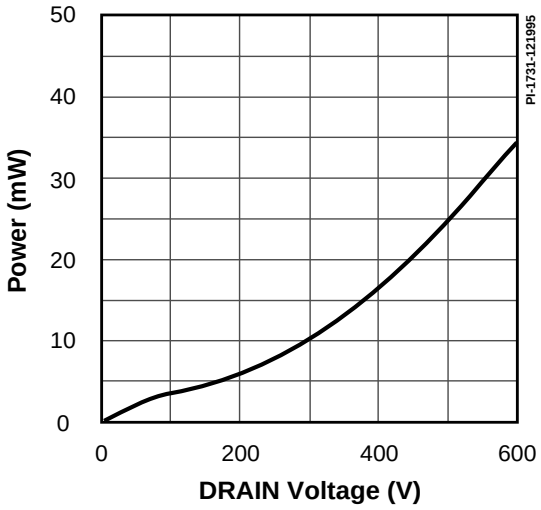
OUTPUT CHARACTERISTIC



C_{OSS} vs. DRAIN VOLTAGE



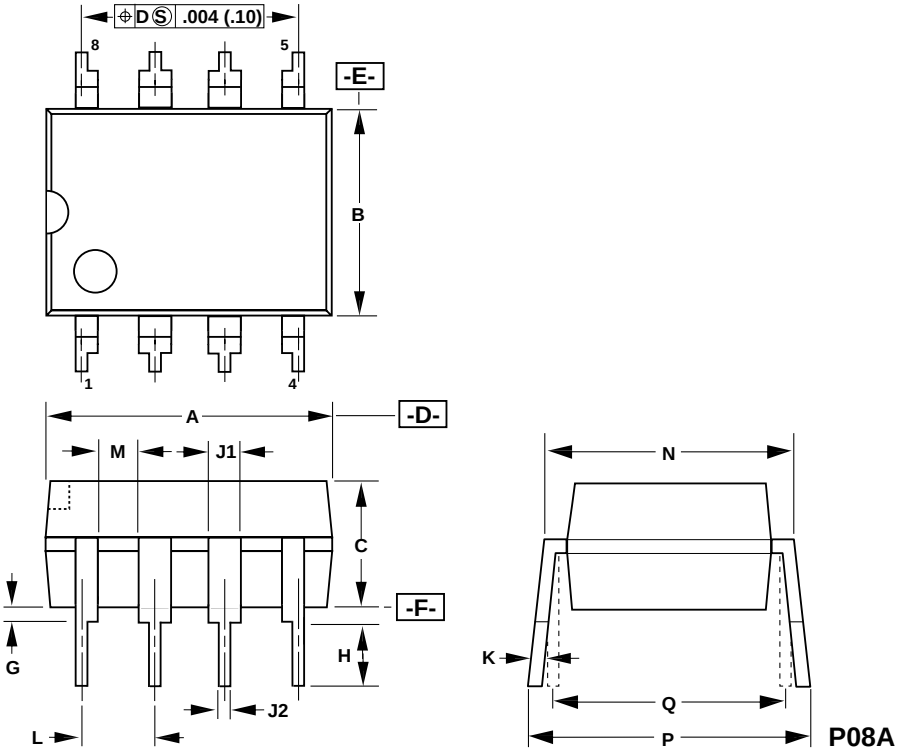
DRAIN CAPACITANCE POWER



DIP-8

DIM	inches	mm
A	0.370-0.385	9.40-9.78
B	0.245-0.255	6.22-6.48
C	0.125-0.135	3.18-3.43
G	0.015-0.040	0.38-1.02
H	0.120-0.135	3.05-3.43
J1	0.060 (NOM)	1.52 (NOM)
J2	0.014-0.022	0.36-0.56
K	0.010-0.012	0.25-0.30
L	0.090-0.110	2.29-2.79
M	0.030 (MIN)	0.76 (MIN)
N	0.300-0.320	7.62-8.13
P	0.300-0.390	7.62-9.91
Q	0.300 BSC	7.62 BSC

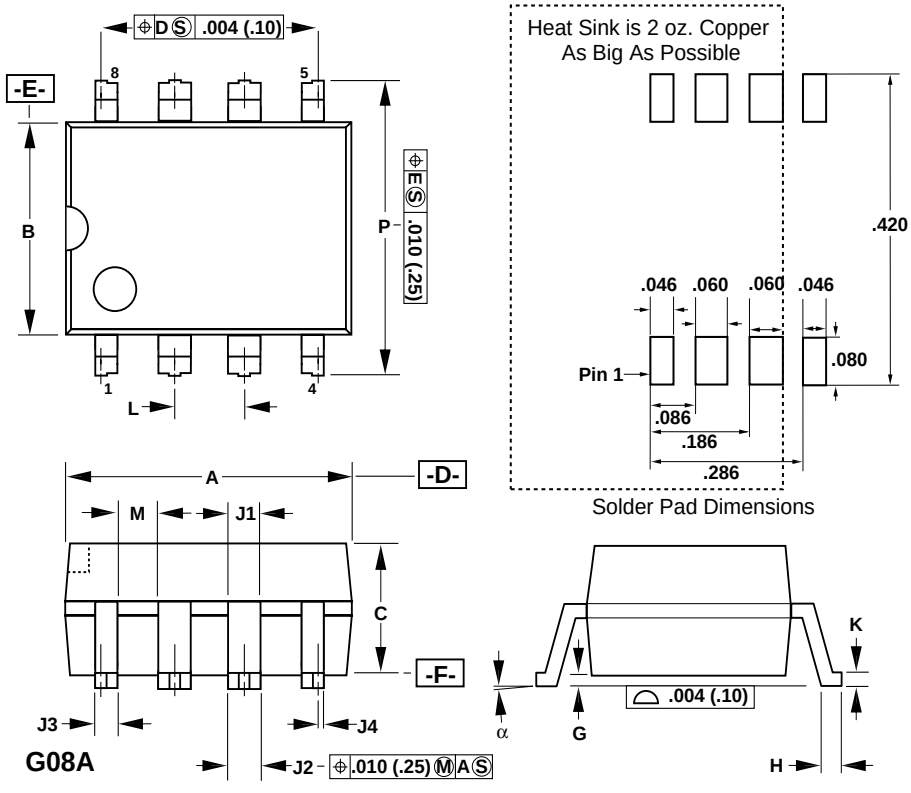
Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 8 leads (issue B, 7/85)..
2. Controlling dimensions are inches.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. D, E and F are reference datums on the molded body.



P08A

PI-2076-041101

SMD-8



DIM	inches	mm
A	0.370-0.385	9.40-9.78
B	0.245-0.255	6.22-6.48
C	0.125-0.135	3.18-3.43
G	0.004-0.012	0.10-0.30
H	0.036-0.044	0.91-1.12
J1	0.060 (NOM)	1.52 (NOM)
J2	0.048-0.053	1.22-1.35
J3	0.032-0.037	0.81-0.94
J4	0.007-0.011	0.18-0.28
K	0.010-0.012	0.25-0.30
L	0.100 BSC	2.54 BSC
M	0.030 (MIN)	0.76 (MIN)
P	0.372-0.388	9.45-9.86
α	0-8°	0-8°

Notes:
1. Package dimensions conform to JEDEC specification MS-001-AB (issue B, 7/85) except for lead shape and size.
2. Controlling dimensions are inches.
3. Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.
4. D, E and F are reference datums on the molded body.

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