Unitrode Products
from Texas Instruments

application INFO available

UC2906
UC3906

Sealed Lead-Acid Battery Charger

FEATURES

- Optimum Control for Maximum Battery Capacity and Life
- Internal State Logic Provides Three Charge States
- Precision Reference Tracks Battery Requirements Over Temperature
- Controls Both Voltage and Current at Charger Output
- System Interface Functions
- Typical Standby Supply Current of only 1.6mA

DESCRIPTION

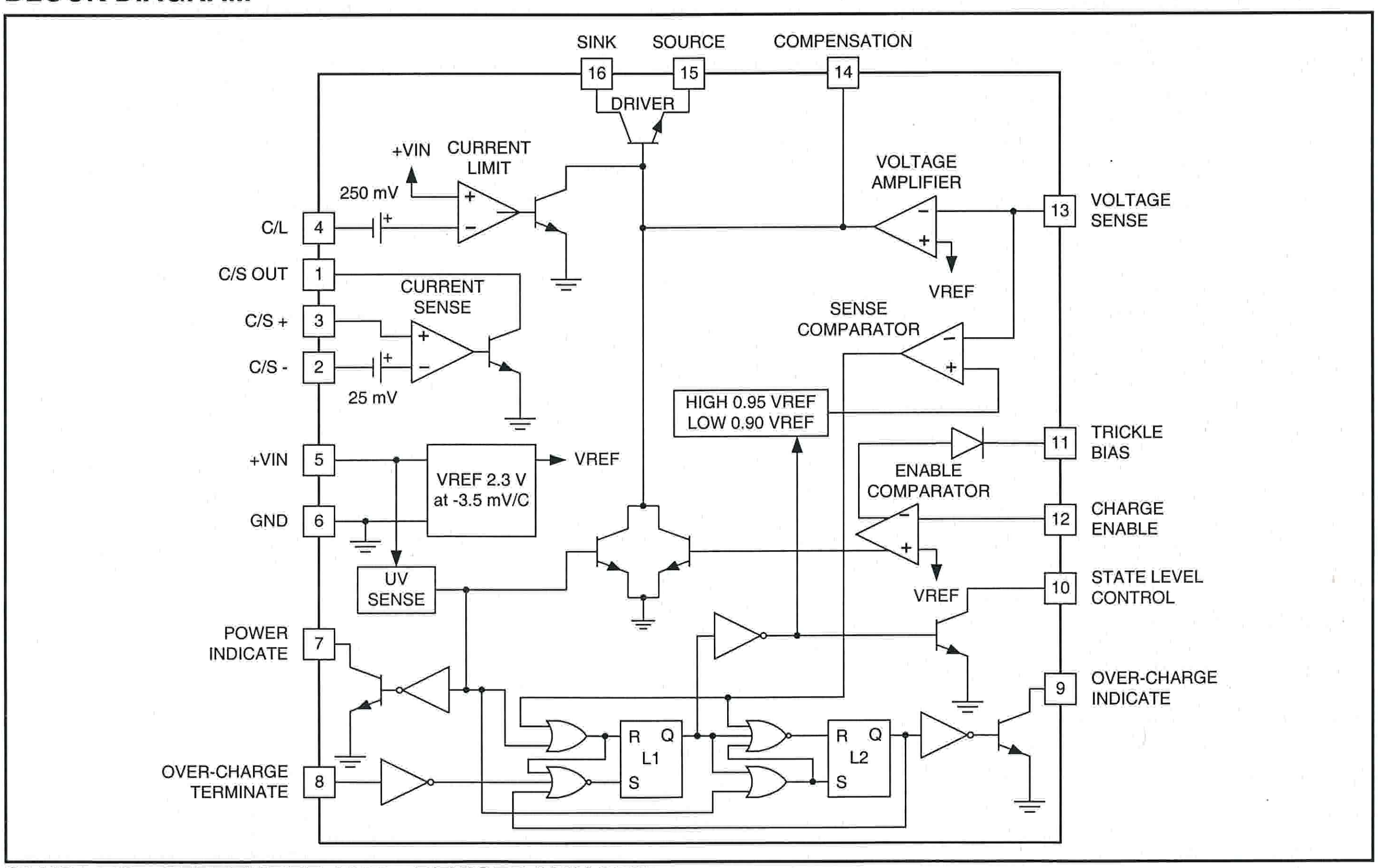
The UC2906 series of battery charger controllers contains all of the necessary circuitry to optimally control the charge and hold cycle for sealed lead-acid batteries. These integrated circuits monitor and control both the output voltage and current of the charger through three separate charge states; a high current bulk-charge state, a controlled over-charge, and a precision float-charge, or standby, state.

Optimum charging conditions are maintained over an extended temperature range with an internal reference that tracks the nominal temperature characteristics of the lead-acid cell. A typical standby supply current requirement of only 1.6mA allows these ICs to predictably monitor ambient temperatures.

Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver. The driver will supply at least 25mA of base drive to an external pass device. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. A charge enable comparator with a trickle bias output can be used to implement a low current turn-on mode of the charger, preventing high current charging during abnormal conditions such as a shorted battery cell.

Other features include a supply under-voltage sense circuit with a logic output to indicate when input power is present. In addition the over-charge state of the charger can be externally monitored and terminated using the over-charge indicate output and over-charge terminate input.

BLOCK DIAGRAM

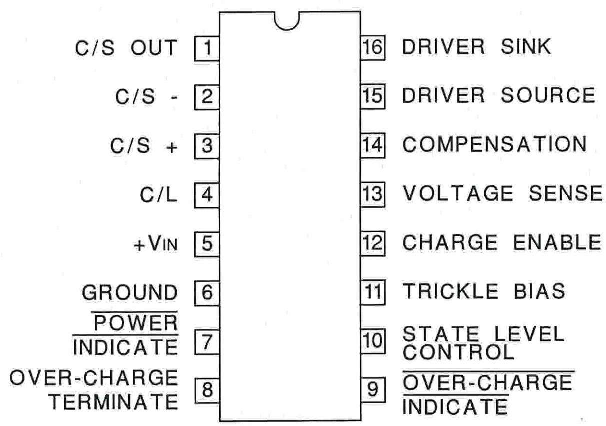


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (+VIN) 40V
Open Collector Output Voltages 40V
Amplifier and Comparator Input Voltages . . . . . . –0.3V to +40V
Over-Charge Terminate Input Voltage . . . . –0.3V to +40V
Current Sense Amplifier Output Current. 80mA
Other Open Collector Output Currents 20mA
Trickle Bias Voltage Differential with respect to VIN . . . . . –32V
Trickle Bias Output Current . . . . –40mA
Driver Current. 80mA
Power Dissipation at T_A = 25°C (Note 2). 1000mW
Power Dissipation at T_C = 25°C (Note 2). 2000mW
Operating Junction Temperature . . . . –55°C to +150°C
Storage Temperature . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) . . . . 300°C

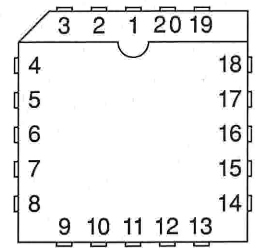
Note 1: *Voltages are referenced to ground (Pin 6). Currents are positive into, negative out of, the specified terminals.*
Note 2: *Consult Packaging section of Databook for thermal limitations and considerations of packages.*

DIL-16, SOIC-16 (TOP VIEW)
J or N Package, DW Package



CONNECTION DIAGRAMS

PLCC-20, LCC-20 (TOP VIEW)
Q, L Packages



PIN FUNCTION	PIN
N/C	1
C/S OUT	2
C/S-	3
C/S+	4
C/L	5
N/C	6
+VIN	7
GROUND	8
POWER INDICATE	9
OVER CHARGE TERMINATE	10
N/C	11
OVER CHARGE INDICATE	12
STATE LEVEL CONTROL	13
TRICKLE BIAS	14
CHARGE ENABLE	15
N/C	16
VOLTAGE SENSE	17
COMPENSATION	18
DRIVER SOURCE	19
DRIVER SINK	20

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for T_A = –40°C to +70°C for the UC2906 and 0°C to +70°C for the UC3906, $+V_{IN}$ = 10V, $T_A = T_J$.

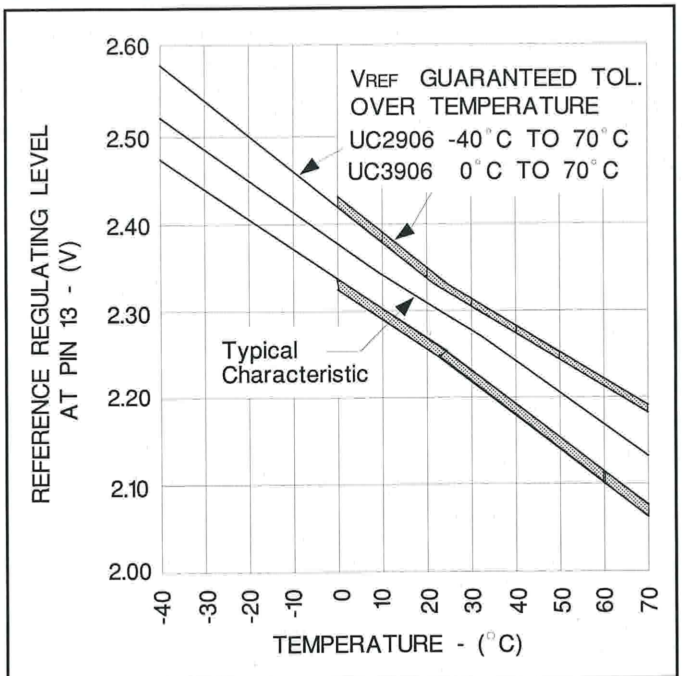
PARAMETER	TEST CONDITIONS	UC2906			UC3906			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Supply								
Supply Current	$+V_{IN}$ = 10V		1.6	3.3		1.6	3.3	mA
	$+V_{IN}$ = 40V		1.8	3.6		1.8	3.6	mA
	$+V_{IN}$ = 40V, T_A = –40°C to 85°C		1.8	4				mA
Supply Under-Voltage Threshold	$+V_{IN}$ = Low to High	4.2	4.5	4.8	4.2	4.5	4.8	V
Supply Under-Voltage Hysteresis			0.20	0.30		0.20	0.30	V
Internal Reference (VREF)								
Voltage Level (Note 3)	Measured as Regulating Level at Pin 13 w/ Driver Current = 1mA, T_J = 25°C	2.275	2.3	2.325	2.270	2.3	2.330	V
Line Regulation	$+V_{IN}$ = 5 to 40V		3	8		3	8	mV
Temperature Coefficient			–3.5			–3.5		mV/°C

ELECTRICAL CHARACTERISTICS: Unless otherwise stated, these specifications apply for $T_A = -40°C$ to $+70°C$ for the UC2906 and 0°C to +70°C for the UC3906, $+V_{IN} = 10V$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC2906			UC3906			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Amplifier								
Input Bias Current	Total Input Bias at Regulating Level	–0.5	–0.2		–0.5	–0.2		µA
Maximum Output Current	Source	–45	–30	–15	–45	–30	–15	µA
	Sink	30	60	90	30	60	90	µA
Open Loop Gain	Driver current = 1mA	50	65		50	65		dB
Output Voltage Swing	Volts above GND or below $+V_{IN}$		0.2			0.2		V
Driver								
Minimum Supply to Source Differential	Pin 16 = $+V_{IN}$, I_O = 10mA		2.0	2.2		2.0	2.2	V
Maximum Output Current	Pin 16 to Pin 15 = 2V	25	40		25	40		mA
Saturation Voltage			0.2	0.45		0.2	0.45	V
Current Limit Amplifier								
Input Bias Current			0.2	1.0		0.2	1.0	µA
Threshold Voltage	Offset below $+V_{IN}$	225	250	275	225	250	275	mV
Threshold Supply Sensitivity	$+V_{IN}$ = 5 to 40V		0.03	0.25		0.03	0.25	%/V
Voltage Sense Comparator								
Threshold Voltage	As a function of V_{REF}, L_1 = RESET	0.94	0.949	0.960	0.94	0.949	0.960	V/V
	As a function of V_{REF}, L_1 = SET	0.895	0.90	0.910	0.895	0.90	0.910	V/V
Input Bias Current	Total Input Bias at Thresholds	–0.5	–0.2		–0.5	–0.2		µA
Current Sense Comparator								
Input Bias Current			0.1	0.5		0.1	0.5	µA
Input Offset Current			0.01	0.2		0.01	0.2	µA
Input Offset Voltage	Referenced to Pin 2, I_{OUT} = 1mA	20	25	30	20	25	30	mV
Offset Supply Sensitivity	$+V_{IN}$ = 5 to 40V		0.05	0.35		0.05	0.35	%/V
Offset Common Mode Sensitivity	CMV = 2V to $+V_{IN}$		0.05	0.35		0.05	0.35	%/V
Maximum Output Current	V_{OUT} = 2V	25	40		25	40		mA
Output Saturation Voltage	I_{OUT} = 10mA		0.2	0.45		0.2	0.45	V
Enable Comparator								
Threshold Voltage	As a function of V_{REF}	0.99	1.0	1.01	0.99	1.0	1.01	V/V
Input Bias Current		–0.5	–0.2		–0.5	–0.2		µA
Trickle Bias Maximum Output Current	$V_{OUT} = +V_{IN} - 3V$	25	40		25	40		mA
Trickle Bias Maximum Output Voltage	Volts below $+V_{IN}$, I_{OUT} = 10mA		2.0	2.6		2.0	2.6	V
Trickle Bias Reverse Hold-Off Voltage	$+V_{IN}$ = 0V, I_{OUT} = –10µA	6.3	7.0		6.3	7.0		V
Over-Charge Terminate Input								
Threshold Voltage		0.7	1.0	1.3	0.7	1.0	1.3	V
Internal Pull-Up Current	At Threshold		10			10		µA
Open Collector Outputs (Pins 7, 9, and 10)								
Maximum Output Current	V_{OUT} = 2V	2.5	5		2.5	5		mA
Saturation Voltage	I_{OUT} = 1.6mA		0.25	0.45		0.25	0.45	V
	I_{OUT} = 50µA		0.03	0.05		0.03	0.05	V
Leakage Current	V_{OUT} = 40V		1	3		1	3	µA

Note 3. The reference voltage will change as a function of power dissipation on the die according to the temperature coefficient of the reference and the thermal resistance, junction-to-ambient.

OPERATION AND APPLICATION INFORMATION



Internal reference temperature characteristic and tolerance.

Dual Level Float Charger Operations

The UC2906 is shown configured as a dual level float charger in Figure 1. All high currents are handled by the external PNP pass transistor with the driver supplying base drive to this device. This scheme uses the TRICKLE BIAS output and the charge enable comparator to give the charger a low current turn on mode. The output current of the charger is limited to a low-level until the battery reaches a specified voltage, preventing a high current charging if a battery cell is shorted. Figure 2 shows the state diagram of the charger. Upon turn on the UV sense circuitry puts the charger in state 1, the high rate bulk-charge state. In this state, once the enable threshold has been exceeded, the charger will supply a peak current that is determined by the 250mV offset in the C/L amplifier and the sensing resistor R_S.

To guarantee full re-charge of the battery, the charger's voltage loop has an elevated regulating level, V_{OC}, during state 1 and state 2. When the battery voltage reaches 95% of V_{OC}, the charger enters the over-charge state, state 2. The charger stays in this state until the OVER-CHARGE TERMINATE pin goes high. In Figure 1, the charger uses the current sense amplifier to generate this signal by sensing when the charge current has tapered to a specified level, I_{OCT}. Alternatively the over-charge could have been controlled by an external source, such as a timer, by using the OVER-CHARGE INDICATE signal at Pin 9. If a load is applied to the battery and begins to discharge it, the charger will contribute its full output to the load. If the battery drops 10% below the float level, the charger will reset itself to state 1. When the load is removed a full charge cycle will follow. A graphical representation of a charge, and discharge, cycle of the dual lever float charger is shown in Figure 3.

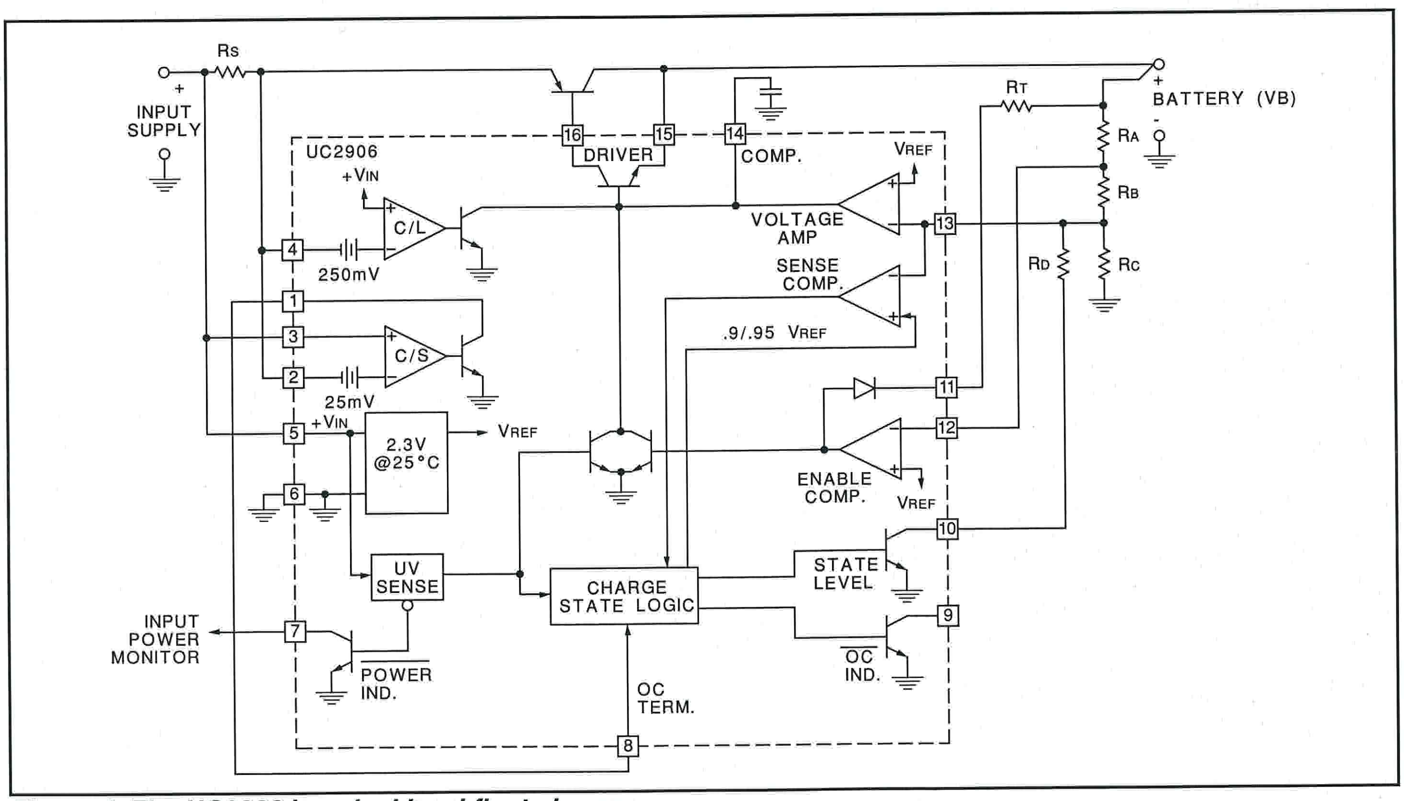


Figure 1. The UC2906 in a dual level float charger.

OPERATION AND APPLICATION INFORMATION (cont.)

Design Procedure

1) *Pick divider current, I_D. Recommended value is 50μA to 100μA.*

2) $R_C = 2.3V / I_D$

3) $R_A + R_B = R_{SUM} = (V_F - 2.3V) / I_D$

4) $R_D = 2.3V \bullet R_{SUM} / (V_{OC} - V_F)$

5) $R_A = (R_{SUM} + R_X)(1 - 2.3V / V_T)$
WHERE: $R_X = R_C \bullet R_D / (R_C + R_D)$

6) $R_B = R_{SUM} - R_A$

7) $R_S = 0.25V / I_{MAX}$

8) $R_T = (V_{IN} - V_T - 2.5V) / I_T$

9) $I_{OCT} = \frac{I_{MAX}}{10}$

Note: $V_{12} = 0.95\, V_{OC}$,
$V_{31} = 0.90\, V_F$,

For further design and application information see UICC Application Note U-104

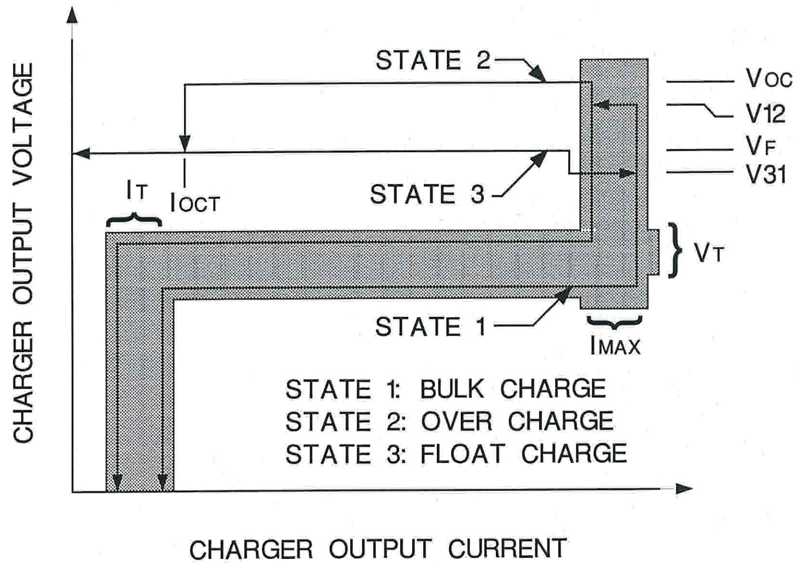
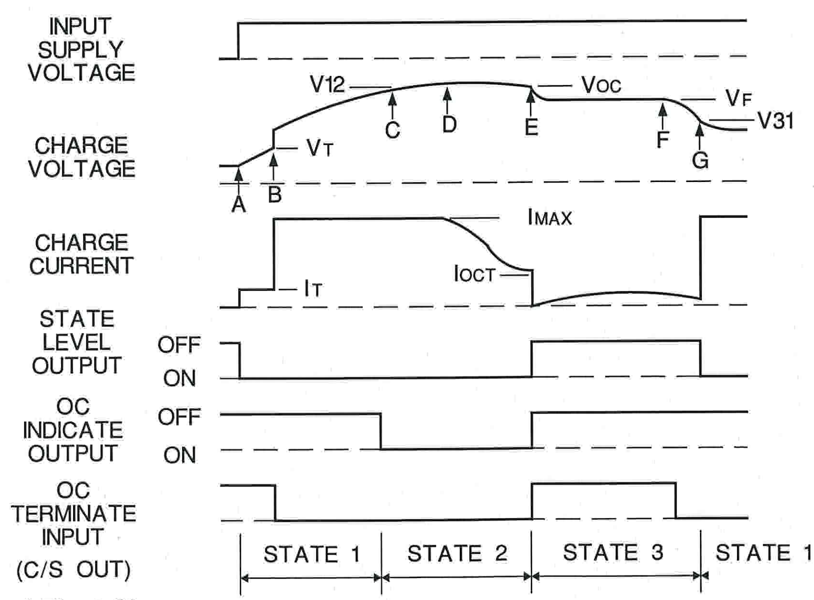


Figure 2. State diagram and design equations for the dual level float charger.



Explanation: Dual Level Float Charger

A. *Input power turns on, battery charges at trickle current rate.*

B. *Battery voltage reaches V_T enabling the driver and turning off the trickle bias output, battery charges at I_{MAX} rate.*

C. *Transition voltage V_{12} is reached and the charger indicates that it is now in the over-charge state, state 2.*

D. *Battery voltage approaches the over-charge level V_{OC} and the charge current begins to taper.*

E. *Charge current tapers to I_{OCT}. The current sense amplifier output, in this case tied to the OC TERMINATE input, goes high. The charger changes to the float state and holds the battery voltage at V_F.*

F. *Here a load (>I_{MAX}) begins to discharge the battery.*

G. *The load discharges the battery such that the battery voltage falls below V_{31}. The charger is now in state 1, again.*

Figure 3. Typical charge cycle: UC2906 dual level float charger.

OPERATION AND APPLICATION INFORMATION (cont.)

Compensated Reference Matches Battery Requirements

When the charger is in the float state, the battery will be maintained at a precise float voltage, V_F. The accuracy of this float state will maximize the standby life of the battery while the bulk-charge and over-charge states guarantee rapid and full re-charge. All of the voltage thresholds on the UC2906 are derived from the internal reference. This reference has a temperature coefficient that tracks the temperature characteristic of the optimum-charge and hold levels for sealed lead-acid cells. This further guarantees that proper charging occurs, even at temperature extremes.

Dual Step Current Charger Operation

Figures 4, 5 and 6 illustrate the UC2906's use in a different charging scheme. The dual step current charger is useful when a large string of series cells must be charged. The holding-charge state maintains a slightly elevated voltage across the batteries with the holding current, 1H. This will tend to guarantee equal charge distribution between the cells. The bulk-charge state is similar to that of the float charger with the exception that when V_{12} is reached, no over-charge state occurs since Pin 8 is tied high at all times. The current sense amplifier is used to regulate the holding current. In some applications a series resistor, or external buffering transistor, may be required at the current sense output to prevent excessive power dissipation on the UC2906.

A PNP Pass Device Reduces Minimum Input to Output Differential

The configuration of the driver on the UC2906 allows a good bit of flexibility when interfacing to an external pass transistor. The two chargers shown in Figures 1 and 4 both use PNP pass devices, although an NPN device driven from the source output of the UC2906 driver can also be used. In situations where the charger must operate with low input to output differentials the PNP pass device should be configured as shown in Figure 4. The PNP can be operated in a saturated mode with only the series diode and sense resistor adding to the minimum differential. The series diode, D1, in many applications, can be eliminated. This diode prevents any discharging of the battery, except through the sensing divider, when the charger is attached to the battery with no input supply voltage. If discharging under this condition must be kept to an absolute minimum, the sense divider can be referenced to the POWER INDICATE pin, Pin 7, instead of ground. In this manner the open collector off state of Pin 7 will prevent the divider resistors from discharging the battery when the input supply is removed.

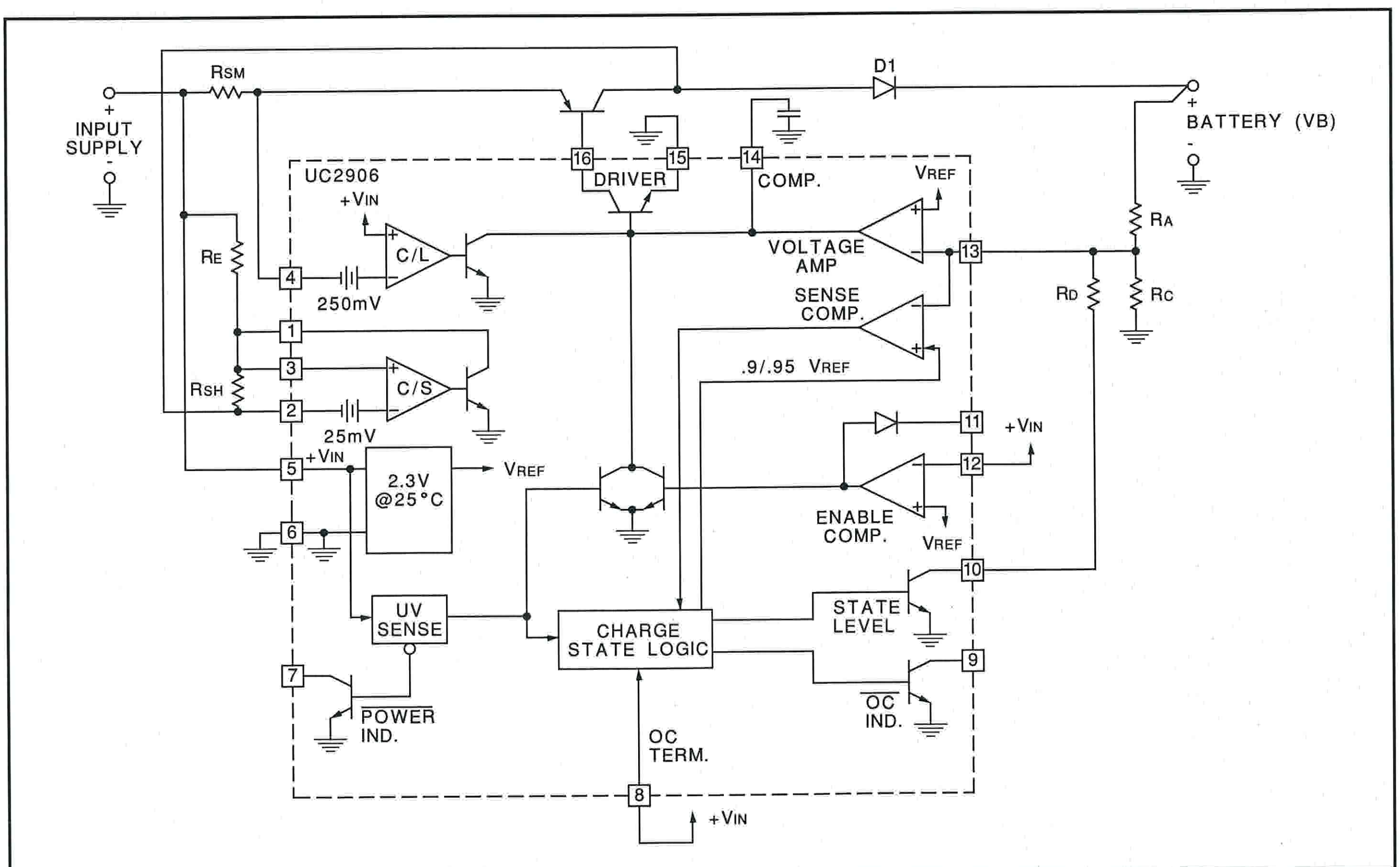
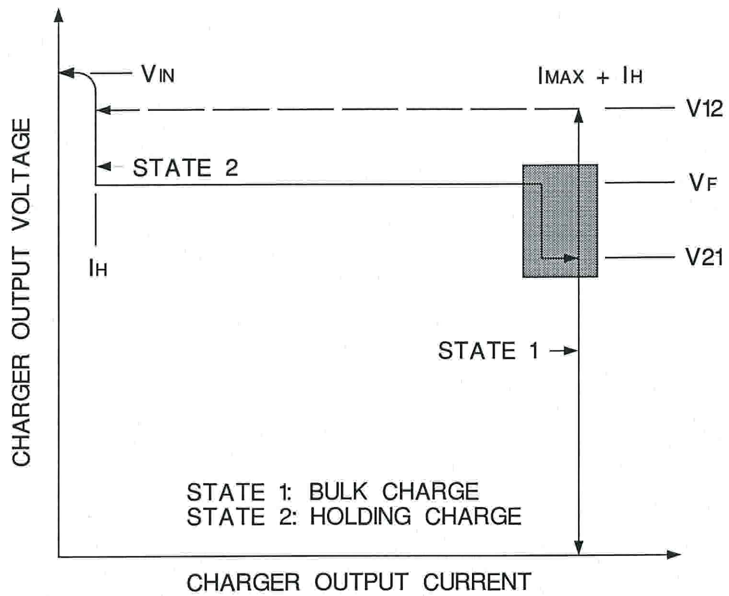


Figure 4. The UC2906 in a dual step current charger.

OPERATION AND APPLICATION INFORMATION (cont.)



1.) $V_{12} = .95\ V_{REF}\left(1 + \frac{R_A}{R_C} + \frac{R_A}{R_D}\right)$

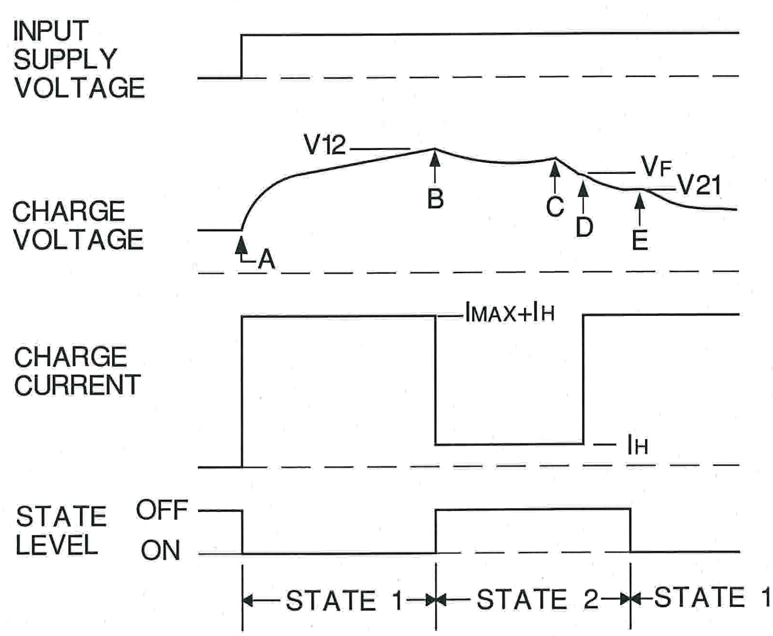
2.) $V_F = V_{REF}\left(1 + \frac{R_A}{R_C}\right)$

3.) $V_{21} = .9\ V_F$

4.) $I_{MAX} = \frac{.25V}{R_{SM}}$

5.) $I_H = \frac{.025V}{R_{SH}}$

Figure 5. State Diagram and design equations for the dual step current charger.



Explanation: Dual Step Current Charger

A. *Input power turns on, battery charges at a rate of $I_H + I_{MAX}$.*

B. *Battery voltage reaches V_{12} and the voltage loop switches to the lower level V_F. The battery is now fed with the holding current I_H.*

C. *An external load starts to discharge the battery.*

D: *When V_F is reached the charger will supply the full current $I_{MAX} + I_H$.*

E. *The discharge continues and the battery voltage reaches V_{21} causing the charger to switch back to state 1.*

Figure 6. Typical charge cycle: UC2906 dual step current charger

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2906DW	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 70	UC2906DW	
UC2906DWG4	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 70	UC2906DW	
UC2906DWTR	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 70	UC2906DW	
UC2906N	NRND	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 70	UC2906N	
UC2906NG4	NRND	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 70	UC2906N	
UC2906Q	NRND	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 70	UC2906Q	
UC3906DW	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-20 to 70	UC3906DW	
UC3906DWG4	NRND	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-20 to 70	UC3906DW	
UC3906DWTR	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-20 to 70	UC3906DW	
UC3906DWTRG4	NRND	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-20 to 70	UC3906DW	
UC3906N	NRND	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-20 to 70	UC3906N	
UC3906NG4	NRND	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-20 to 70	UC3906N	
UC3906Q	NRND	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-20 to 70	UC3906Q	
UC3906QG3	NRND	PLCC	FN	20	46	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-20 to 70	UC3906Q	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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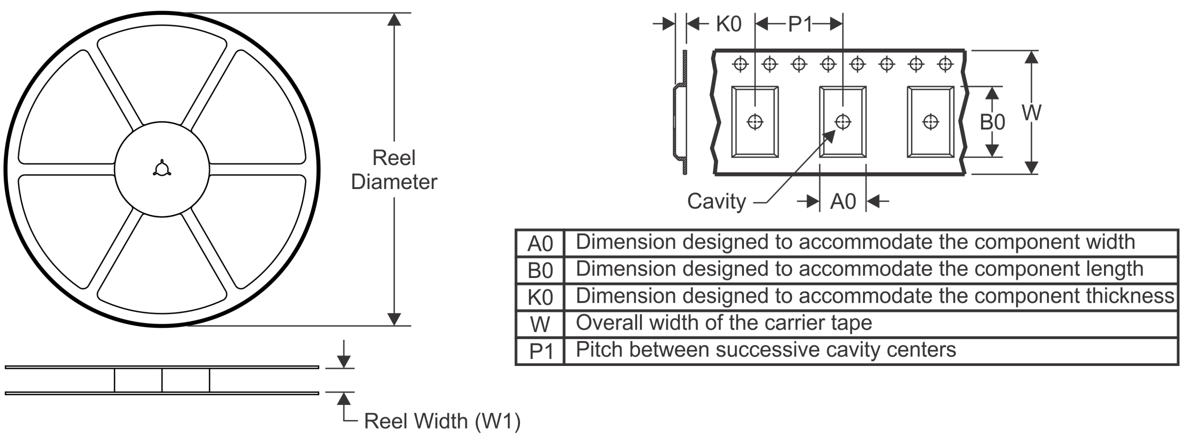
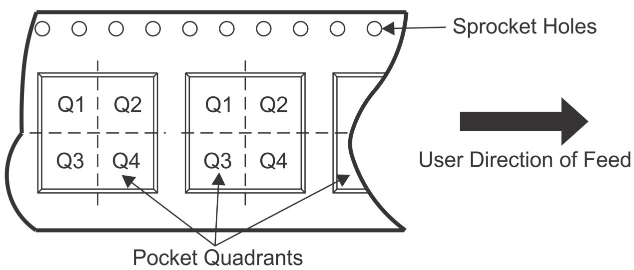
TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

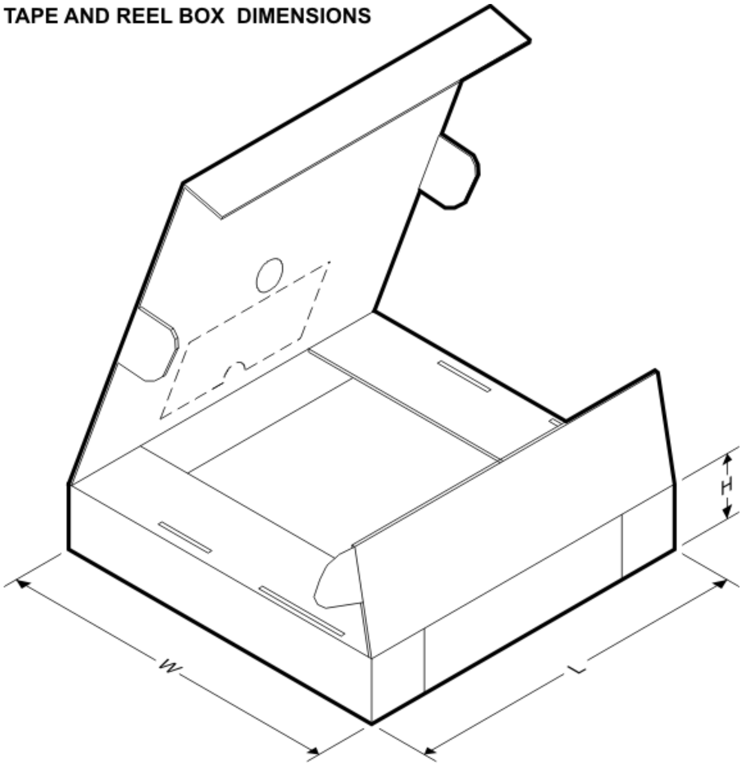
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2906DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UC3906DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

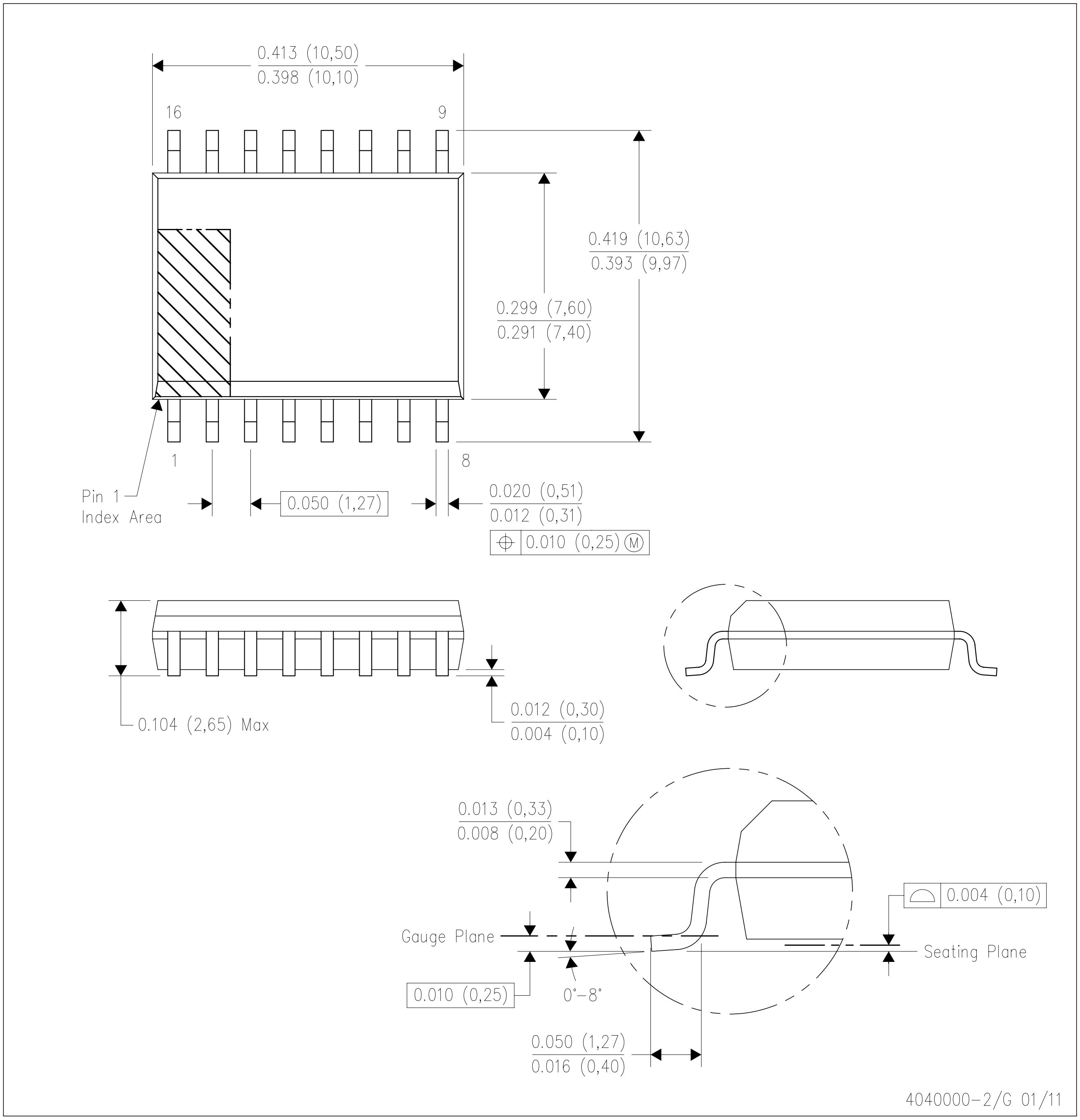
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

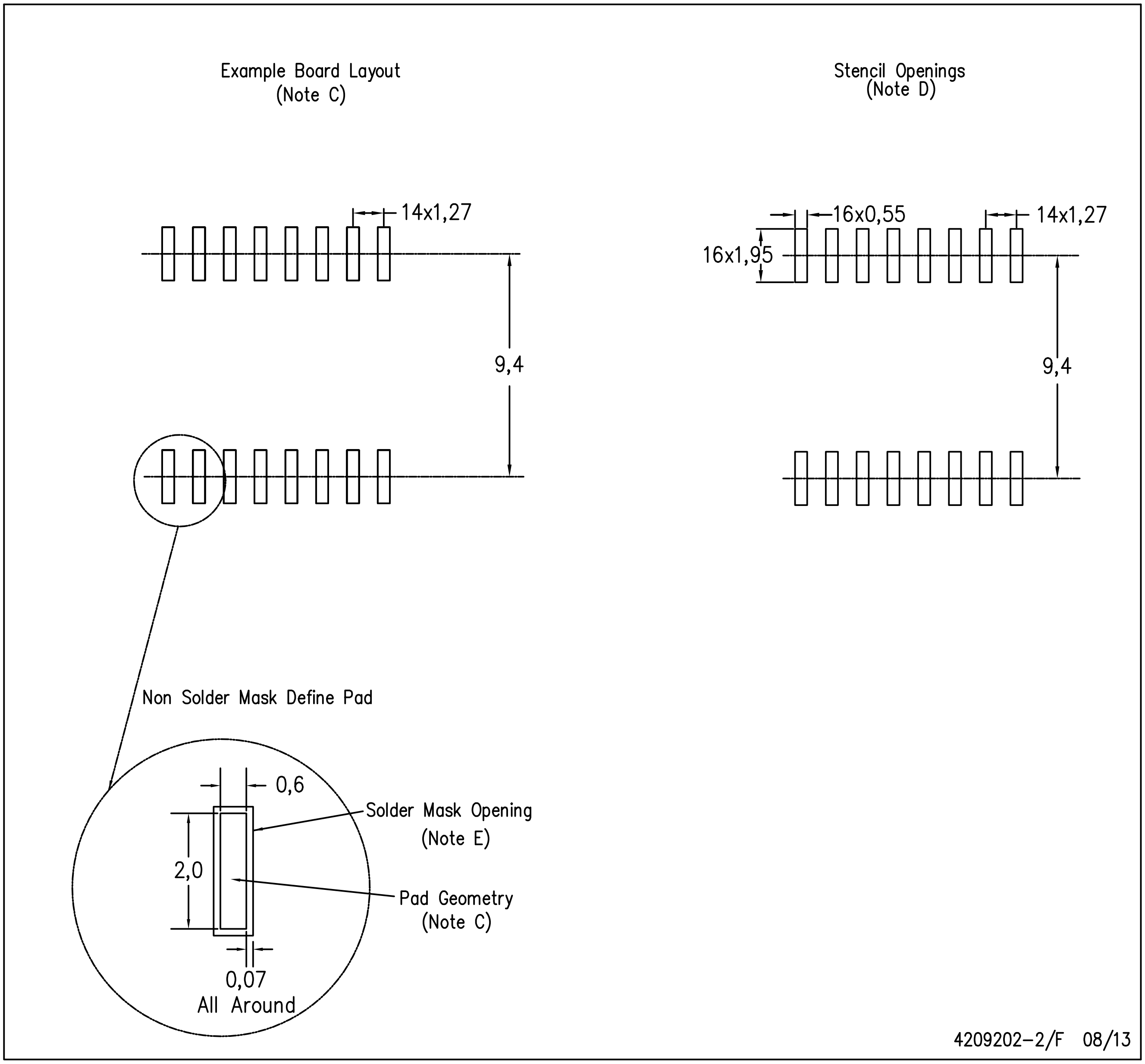
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2906DWTR	SOIC	DW	16	2000	367.0	367.0	38.0
UC3906DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

DW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AA.

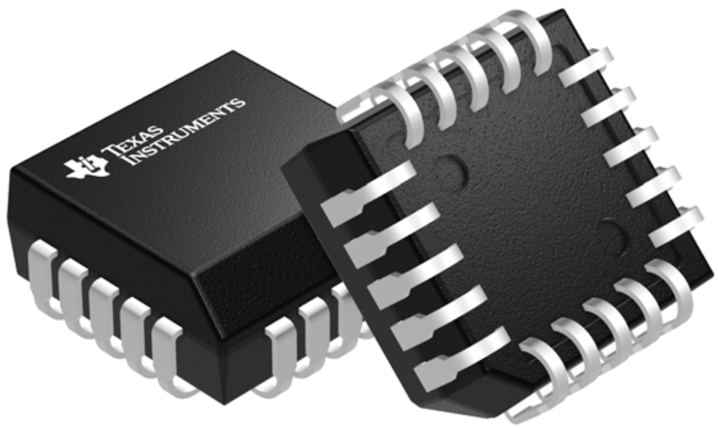
DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

FN 20 PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER

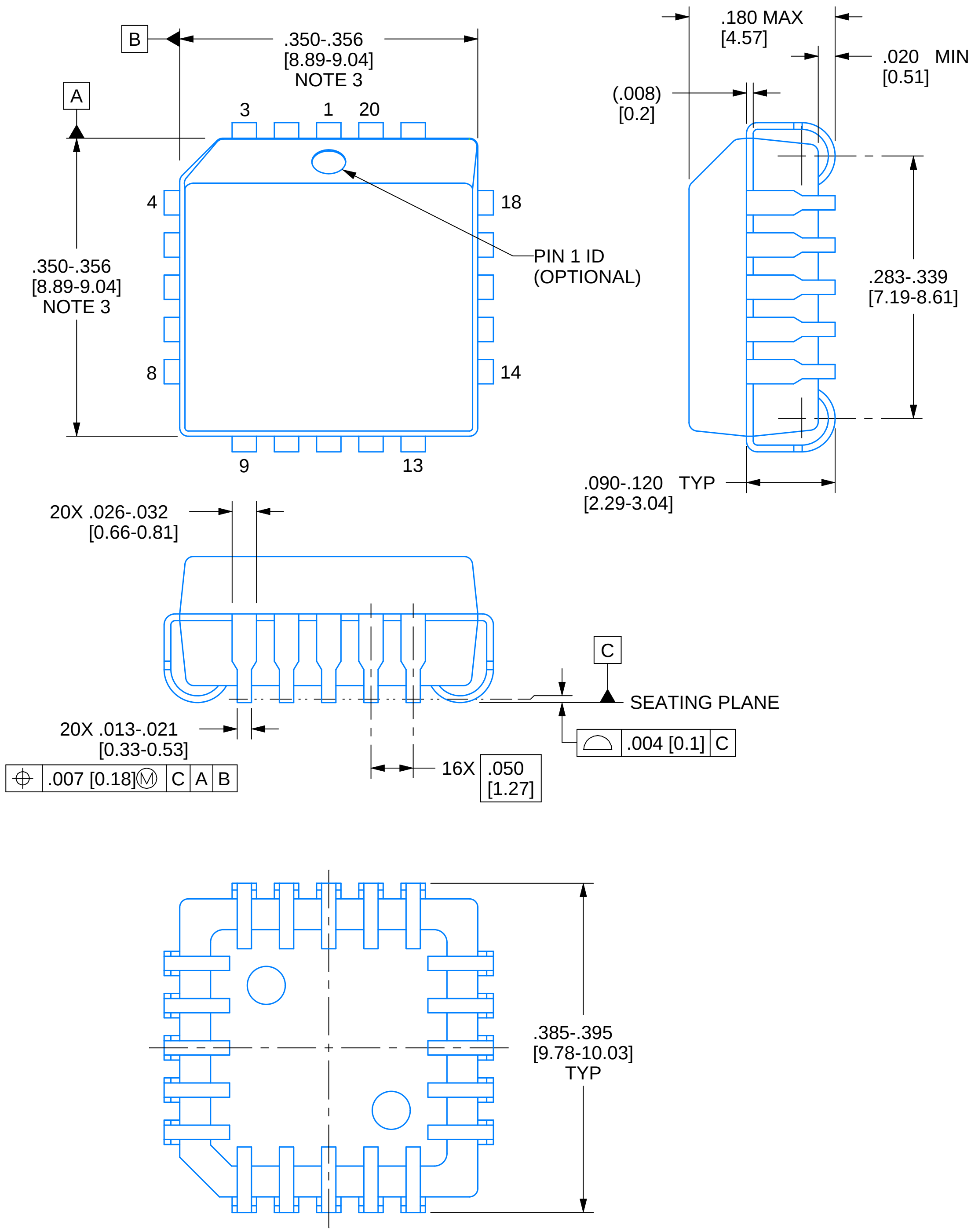


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

PLCC - 4.57 mm max height

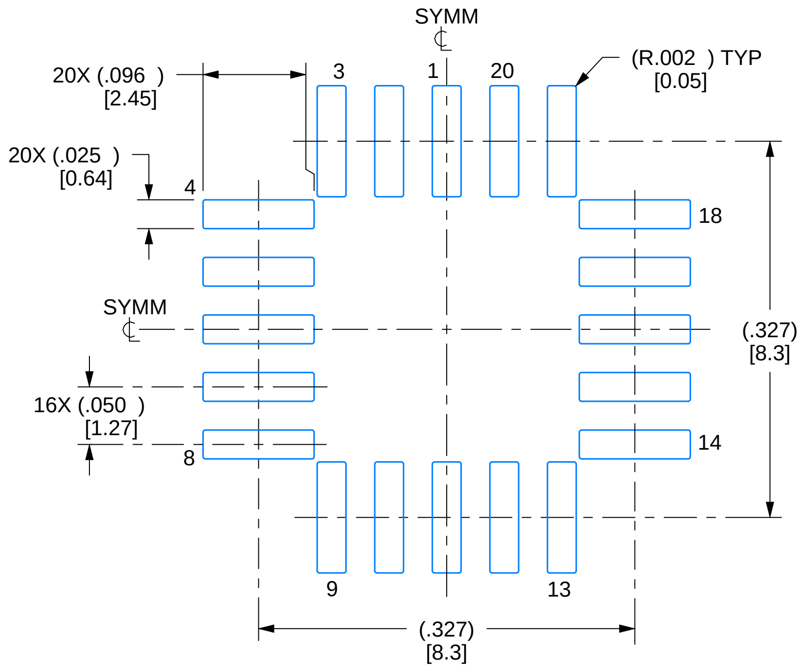
PLASTIC CHIP CARRIER



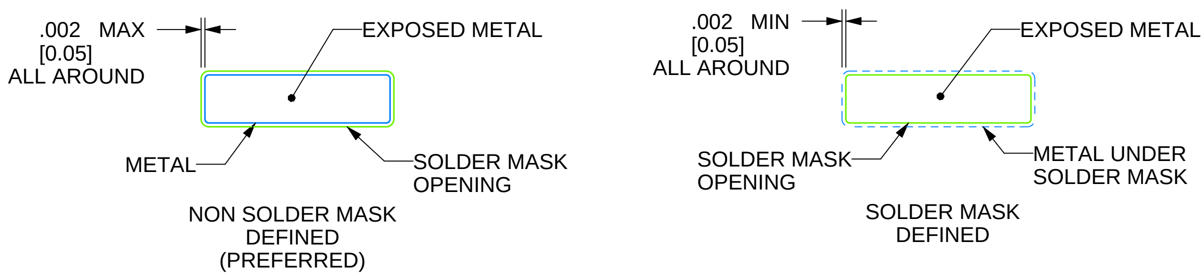
4215152/B 04/2017

NOTES:

1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

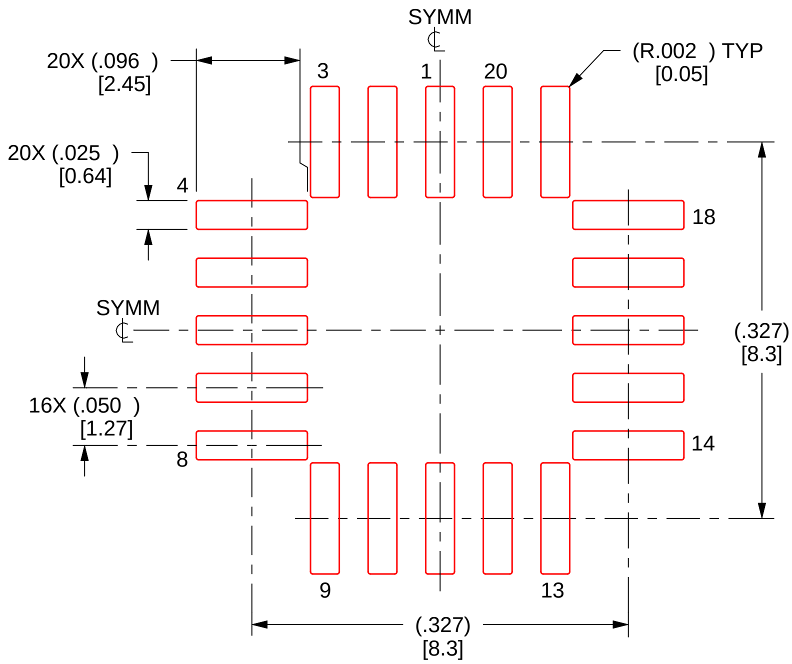


SOLDER MASK DETAILS

4215152/B 04/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

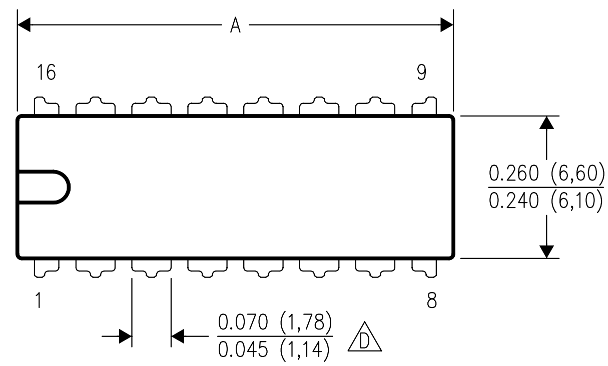
4215152/B 04/2017

NOTES: (continued)

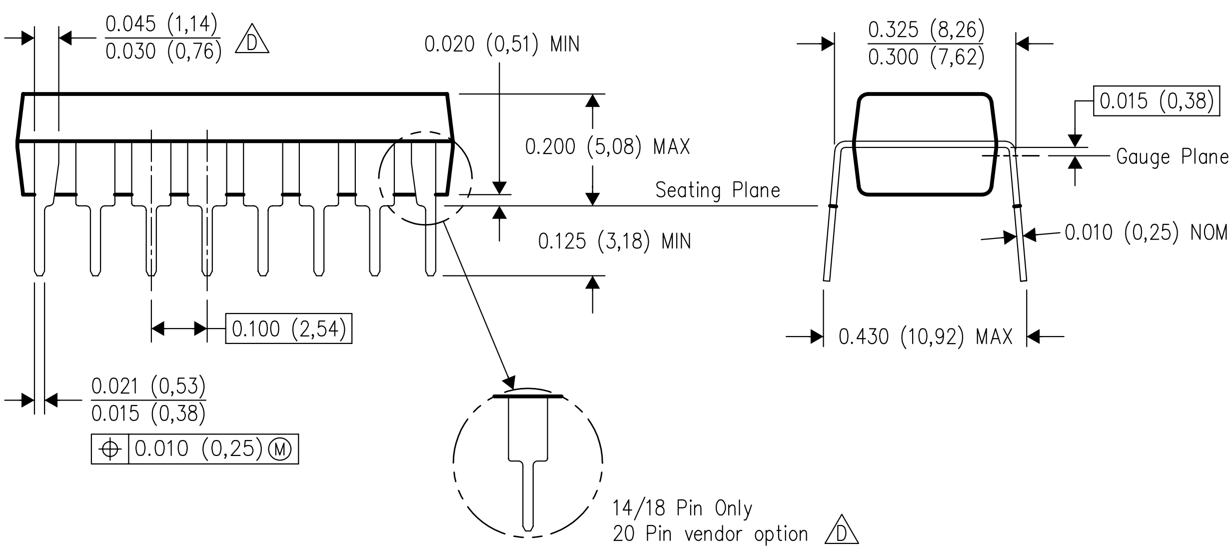
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
(C) MS–001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- (C) Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

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