

# STD25NF10L

# N-CHANNEL 100V - 0.030 Ω - 25A DPAK LOW GATE CHARGE STripFET™ II POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD25NF10L	100 V	< 0.035 Ω	25 A

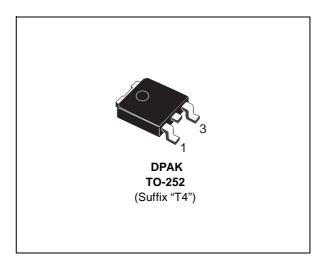
- TYPICAL  $R_{DS}(on) = 0.030 \Omega$
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- LOW THRESHOLD DEVICE
- LOGIC LEVEL DEVICE
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

#### **DESCRIPTION**

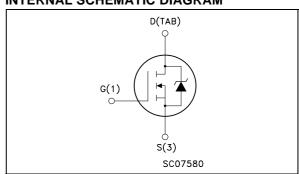
This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced highefficiency, high-frequency isolated DC-DC converters for Telecom and Computer applications. It is also intended for any applications with low gate drive requirements

#### **APPLICATIONS**

- HIGH-EFFICIENCY DC-DC CONVERTERS
- UPS AND MOTOR CONTROL



#### **INTERNAL SCHEMATIC DIAGRAM**



#### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	100	V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	100	V
V <sub>GS</sub>	Gate- source Voltage	± 16	V
I <sub>D</sub> (*)	Drain Current (continuous) at T <sub>C</sub> = 25°C	25	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	25	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	100	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	100	W
	Derating Factor	0.67	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	20	V/ns
E <sub>AS</sub> (2)	Single Pulse Avalanche Energy	450	mJ
T <sub>stg</sub>	Storage Temperature	-55 to 175	°C
Tj	Max. Operating Junction Temperature	-55 to 175	

<sup>(•)</sup> Pulse width limited by safe operating area.
(\*) Current Limited by Package

(2) Starting  $T_j = 25$  °C,  $I_D = 12.5A$ ,  $V_{DD} = 50V$ 

February 2003

<sup>(1)</sup>  $I_{SD} \le 25A$ , di/dt  $\le 300A/\mu s$ ,  $V_{DD} \le V_{(BR)DSS}$ ,  $T_j \le T_{JMAX}$ 

#### THERMAL DATA

Rthj-case Rthj-pcb T <sub>I</sub>	Thermal Resistance Junction-case Thermal Resistance Junction-pcb(#) Maximum Lead Temperature For Soldering Purpose	Max Max	1.5 50 275	°C/W °C/W
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<sup>(#)</sup> When Mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz of Cu.

# **ELECTRICAL CHARACTERISTICS** (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0$	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	$V_{DS} = Max Rating$ $V_{DS} = Max Rating T_C = 125^{\circ}C$			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 16 V			±100	nA

#### ON (\*)

Symbol	Parameter	Test Conditions		Min.	Тур.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$	I <sub>D</sub> = 250 μA	1		2.5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 12.5 A I <sub>D</sub> = 12.5 A		0.030 0.035	0.035 0.040	Ω Ω

#### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	$V_{DS} = 15 \text{ V}$ $I_{D} = 12.5 \text{ A}$		24		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V f = 1 MHz V_{GS} = 0$		1710 250 110		pF pF pF

#### **ELECTRICAL CHARACTERISTICS** (continued)

#### **SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub>	Turn-on Delay Time Rise Time	$\begin{aligned} &V_{DD} = 50 \text{ V} &I_{D} = 12.5 \text{ A} \\ &R_{G} = 4.7 \Omega &V_{GS} = 5 \text{ V} \\ &(\text{Resistive Load, Figure 3}) \end{aligned}$		20 40		ns ns
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V <sub>DD</sub> = 80 V I <sub>D</sub> = 25 A V <sub>GS</sub> = 5 V		38 8.5 21	52	nC nC nC

#### **SWITCHING OFF**

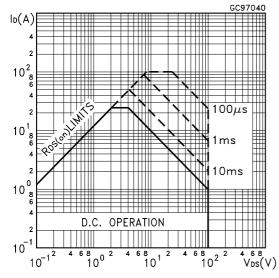
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(off)</sub> t <sub>f</sub>	Turn-off Delay Time Fall Time	$\begin{aligned} &V_{DD} = 50 \text{ V} & I_{D} = 12.5 \text{ A} \\ &R_{G} = 4.7\Omega, & V_{GS} = 5 \text{ V} \\ &(\text{Resistive Load, Figure 3}) \end{aligned}$		58 20		ns ns

#### **SOURCE DRAIN DIODE**

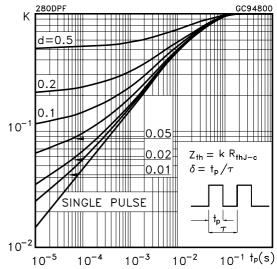
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub> I <sub>SDM</sub> (•)	Source-drain Current Source-drain Current (pulsed)				25 100	A A
V <sub>SD</sub> (*)	Forward On Voltage	I <sub>SD</sub> = 25 A V <sub>GS</sub> = 0			1.5	V
t <sub>rr</sub> Q <sub>rr</sub> IRRM	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 25 \text{ A}$ di/dt = 100A/ $\mu$ s $V_{DD} = 50 \text{ V}$ $T_j = 150^{\circ}\text{C}$ (see test circuit, Figure 5)		88 317 7.2		ns nC A

<sup>(\*)</sup>Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %. (•)Pulse width limited by safe operating area.

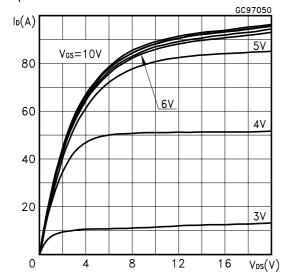
#### Safe Operating Area



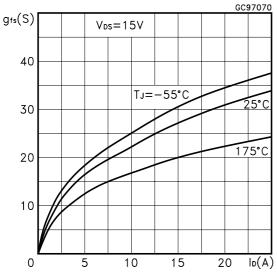
#### Thermal Impedance



#### **Output Characteristics**

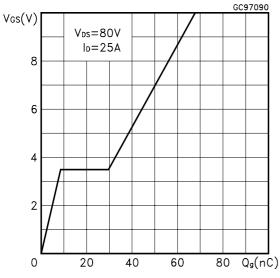


#### Transconductance

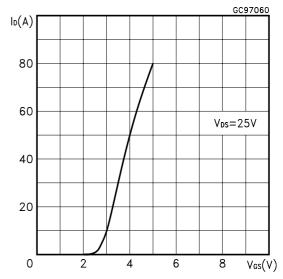


Gate Charge vs Gate-source Voltage

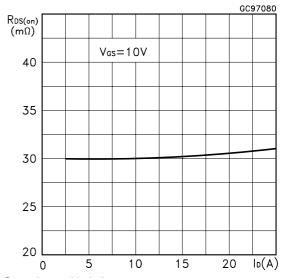
4/9



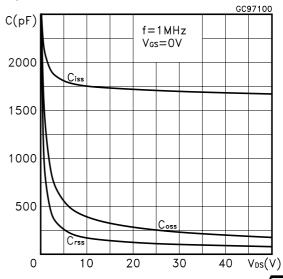
#### **Transfer Characteristics**



#### Static Drain-source On Resistance



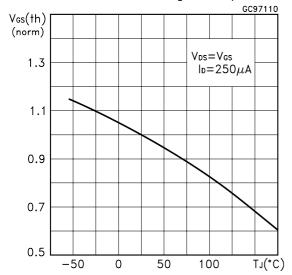
#### Capacitance Variations



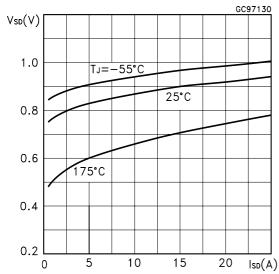
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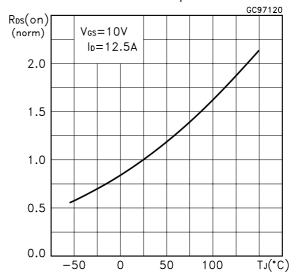
#### Normalized Gate Threshold Voltage vs Temperature



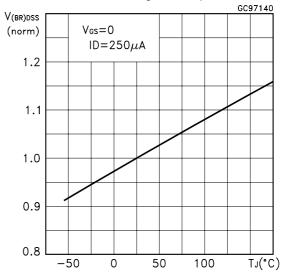
#### Source-drain Diode Forward Characteristics



#### Normalized on Resistance vs Temperature



#### Normalized Breakdown Voltage vs Temperature



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Fig. 1: Unclamped Inductive Load Test Circuit

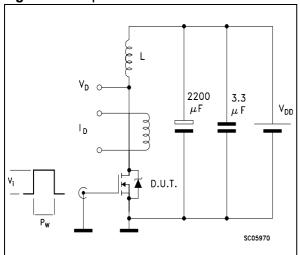
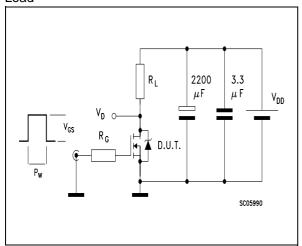


Fig. 3: Switching Times Test Circuits For Resistive Load



**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times

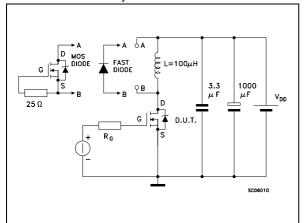


Fig. 2: Unclamped Inductive Waveform

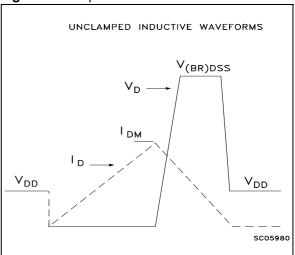
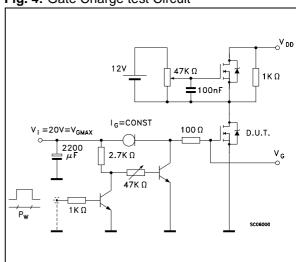
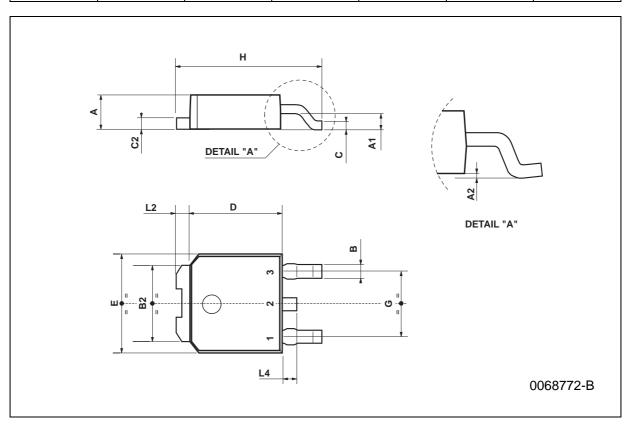


Fig. 4: Gate Charge test Circuit



# **TO-252 (DPAK) MECHANICAL DATA**

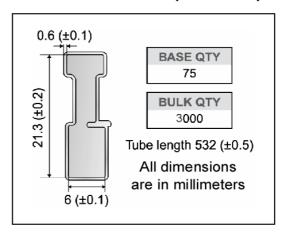
DIM.		mm			inch	
Diwi.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
А	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
В	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
С	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
Е	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
Н	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



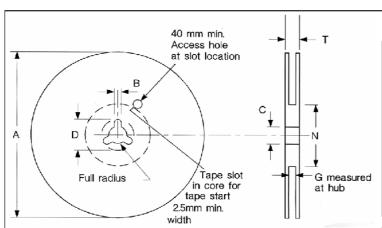
#### **DPAK FOOTPRINT**

# 6.7 1.8 3.0 1.6 2.3 1.6 All dimensions are in millimeters

### **TUBE SHIPMENT (no suffix)\***



## TAPE AND REEL SHIPMENT (suffix "T4")\*

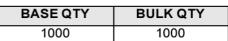


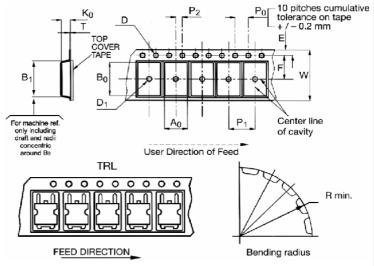
#### REEL MECHANICAL DATA

DIM.	mm		ine	ch
	MIN.	MAX.	MIN.	MAX.
Α		330		12.992
В	1.5		0.059	
С	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
Т		22.4		0.881

TAPE	MECHANICA	ATA L
		$^{1}$

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
В0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641





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