# SN75176A Differential Bus Transceiver

## 1 Features

- Bidirectional Transceiver
- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and ITU Recommendations V.11
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability ±60 mA Max
- Thermal-Shutdown Protection
- Driver Positive-Current Limiting and Negative-Current Limiting
- Receiver Input Impedance 12 kΩ Min
- Receiver Input Sensitivity ±200 mV
- Receiver Input Hysteresis 50 mV Typ
- Operates From Single 5-V Supply
- Lower Power Requirements

## 2 Applications

- Low Speed RS485 communication (5 Mbps or less)
- For 10 Mbps, use SN75176B

## 3 Description

The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The SN75176A combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or VCC = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN75176A can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

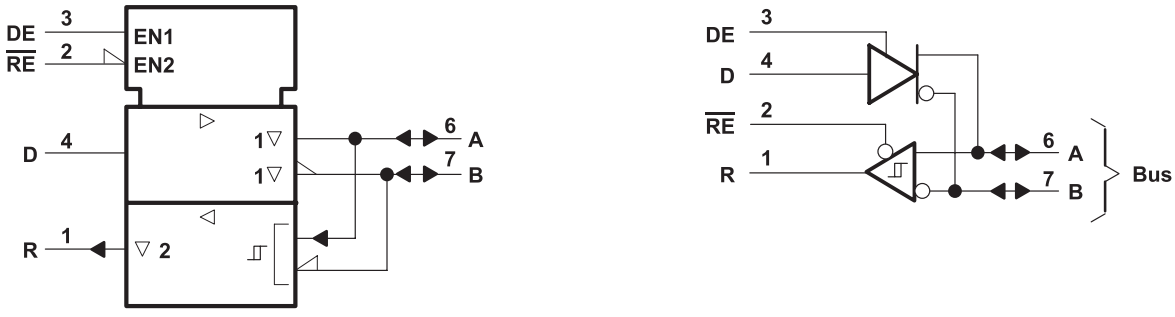
The SN75176A is characterized for operation from 0°C to 70°C.

**Device Information**(1)

| PART NUMBER | PACKAGE (PIN) | BODY SIZE (NOM) |
|---|---|---|
| SN75176A | SOIC (8) | 4.90 mm × 3.91 mm |
| | PDIP (8) | 9.81 mm × 6.35 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

**Simplified Schematics**



## Table of Contents



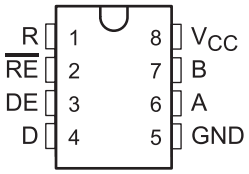
## 4 Revision History

**Changes from Revision May (1995) to Revision B** **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1

# 5 Pin Configuration and Functions

**D OR P PACKAGE**
**(TOP VIEW)**




**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| R | 1 | O | Logic Data Output from RS-485 Receiver |
| $\overline{RE}$ | 2 | I | Receive Enable (active low) |
| DE | 3 | I | Driver Enable (active high) |
| D | 4 | I | Logic Data Input to RS-485 Driver |
| GND | 5 | — | Device Ground Pin |
| A | 6 | I/O | RS-422 or RS-485 Data Line |
| B | 7 | I/O | RS-422 or RS-485 Data Line |
| $V_{CC}$ | 8 | — | Power Input. Connect to 5-V Power Source. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage(2) | | 7 | V |
| | Voltage range at any bus terminal | –10 | 15 | V |
| $V_I$ | Enable input voltage | | 5.5 | V |
| | Continuous Total power Dissipation | See Table 1 | | |
| $T_A$ | Operating free-air temperature range | 0 | 70 | °C |
| $T_{stg}$ | Storage temperature range | 65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±XXX | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±YYY | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| $V_I$ or $V_{IC}$ | Voltage at any buss terminal (separately or common mode) | | –7 | | 12 | V |
| $V_{IH}$ | High-level input voltage | D, DE, and $\overline{RE}$ | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | D, DE, and $\overline{RE}$ | | | 0.8 | V |
| $V_{ID}$ | Differential input voltage(1) | | | | ±12 | V |
| $I_{OH}$ | High-level output current | Driver | | | –60 | mA |
| | | Receiver | | | –400 | µA |
| $I_{OL}$ | Low-level output current | Driver | | | 60 | mA |
| | | Receiver | | | 8 | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

(1) Differential-input/output bus voltage is measured at the non-inverting terminal A with respect to the inverting terminal B.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | SN75176A | | UNIT |
|---|---|---|---|---|
| | | D | P | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 172 | 113 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

**Table 1. Dissipation Rating Table**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING |
|---|---|---|---|
| D | 725 mW | 5.8 mW/°C | 464 mW |
| P | 1100 mW | 8.8 mW/°C | 704 mW |

## 6.5 Electrical Characteristics – Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $I_I$ = –18 mA | | | | –1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = –33 mA | | | 3.7 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = 33 mA | | | 1.1 | | V |
| $\|V_{OD1}\|$ | Differential output voltage | $I_O$ = 0 | | | | $2V_{OD2}$ | V |
| $\|V_{OD2}\|$ | Differential output voltage | RL = 100 Ω, see Figure 8 | | 2 | 2.7 | | V |
| | | RL = 54 Ω, see Figure 8 | | 1.5 | 2.4 | | |
| $\Delta\|V_{OD}\|$ | Change in magnitude of differential output voltage(2) | | | | | ±0.2 | V |
| $V_{OC}$ | Common-mode output voltage(3) | RL = 54 Ω or 100 Ω, see Figure 8 | | | | 3 | V |
| $\Delta\|V_{OC}\|$ | Change in magnitude of common-mode output voltage(2) | | | | | ±0.2 | V |
| $I_O$ | Output current | Output disabled(4) | $V_O$ = 12 V | | | 1 | mA |
| | | | $V_O$ = –7 V | | | –0.8 | |
| $I_{IH}$ | High-level input current | $V_I$ = 2.4 V | | | | 20 | µA |
| $I_{IL}$ | Low-level input current | $V_I$ = 0.4 V | | | | –400 | µA |
| $I_{OS}$ | Short-circuit output current | $V_O$ = –7 V | | | | –250 | mA |
| | | $V_O$ = $V_{CC}$ | | | | 250 | |
| | | $V_O$ = 12 V | | | | 500 | |
| $I_{CC}$ | Supply current (total package) | No load | Outputs enabled | | 35 | 50 | mA |
| | | | Outputs disabled | | 26 | 40 | |

(1) All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
(2) $\Delta|V_{OD}|$ and $D|V_{OC}|$ are the changes in magnitude of $V_{OD}$ and $V_{OC}$ respectively, that occur when the input is changed from a high level to a low level.
(3) In ANSI Standard EIA/TIA-422-B, $V_{OC}$, which is the average of the two output voltages with respect to GND, is called output offset voltage, $V_{OS}$.
(4) This applies for both power on and off; refer to ANSI Standard EIA/TIA-422-B for exact conditions.

## 6.6 Electrical Characteristics – Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | $V_O$ = 2.7 V, $I_O$ = –0.4 mA | | | | 0.2 | V |
| $V_{IT–}$ | Negative-going input threshold voltage | $V_O$ = 0.5 V, $I_O$ = 8 mA | | –0.2 | | | V |
| $V_{hys}$ | Input hysteresis voltage ($V_{IT}$+ – $V_{IT-}$) | | | | 50 | | mV |
| $V_{IK}$ | Enable clamp voltage | $I_I$ = –18 mA | | | | –1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{ID}$ = 200 mV, $I_{OH}$ = –400 µA See Figure 9 | | 2.7 | | | V |
| $V_{OL}$ | Low-level output voltage | $V_{ID}$ = 200 mV, $I_{OH}$ = 8 mA See Figure 9 | | | | 0.45 | V |
| $I_{OZ}$ | High-impedance-state output current | $V_O$ = 0.4 V to 2.4 V | | | | ±20 | µA |
| $I_I$ | Line input current | Other input = 0 V(2) | $V_I$ = 12 V | | | 1 | mA |
| | | | $V_I$ = –7 V | | | –0.8 | |
| $I_{IH}$ | High-level enable input current | $V_{IH}$ = 2.7 V | | | | 20 | µA |
| $I_{IL}$ | Low-level enable input current | $V_{IL}$ = 0.4 V | | | | –100 | µA |
| $r_i$ | Input resistance | | | 12 | | | kΩ |
| $I_{OS}$ | Short-circuit output current | | | –15 | | –85 | mA |
| $I_{CC}$ | Supply current (total package) | No load | Outputs enabled | | 35 | 50 | mA |
| | | | Outputs disabled | | 26 | 40 | |

(1) All typical values are at $V_{CC}$ = 5 V, TA = 25°C.
(2) This applies for both power on and power off. Refer to ANSI Standard EIA/TIA-422-B for exact conditions.

## 6.7 Switching Characteristics – Driver

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{d(OD)}$ | Differential-output delay time | $R_L$ = 60 Ω, See Figure 10 | | 40 | 60 | ns |
| $t_{t(OD)}$ | Differential-output transition time | | | 65 | 95 | ns |
| $t_{PZH}$ | Output enable time to high level | $R_L$ = 110 Ω, See Figure 11 | | 55 | 90 | ns |
| $t_{PZL}$ | Output enable time to low level | $R_L$ = 110 Ω, See Figure 12 | | 30 | 50 | ns |
| $t_{PHZ}$ | Output disable time form high level | $R_L$ = 110 Ω, See Figure 11 | | 85 | 130 | ns |
| $t_{PLZ}$ | Output disable time from low level | $R_L$ = 110 Ω, See Figure 12 | | 20 | 40 | ns |

## 6.8 Switching Characteristics – Receiver

$V_{CC}$ = 5 V, $C_L$ = 15 pF, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $V_{ID}$ = –1.5 V to 1.5 V, See Figure 13 | | 21 | 35 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | | 23 | 35 | ns |
| $t_{PZH}$ | Output enable time to high level | See Figure 14 | | 10 | 30 | ns |
| $t_{PZL}$ | Output enable time to low level | | | 12 | 30 | ns |
| $t_{PHZ}$ | Output disable time from high level | See Figure 14 | | 20 | 35 | ns |
| $t_{PLZ}$ | Output disable time from low level | | | 17 | 25 | ns |

## 6.9 Typical Characteristics

Conditions listed in each chart

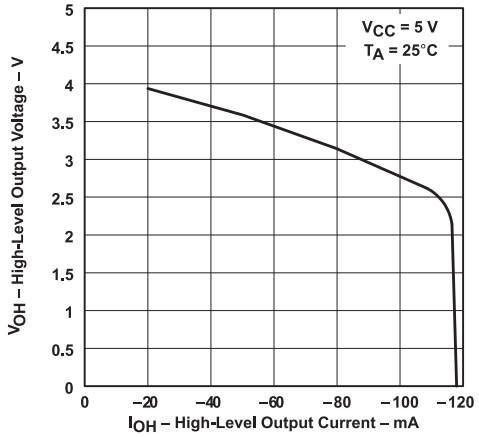



**Figure 1. Driver, High-level Output Voltage vs High-Level Output Current**

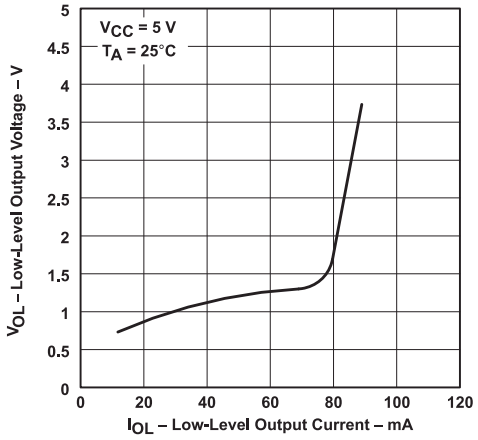



**Figure 2. Driver, Low-Level Output Voltage vs Low-Level Output Current**

## Typical Characteristics (continued)

Conditions listed in each chart

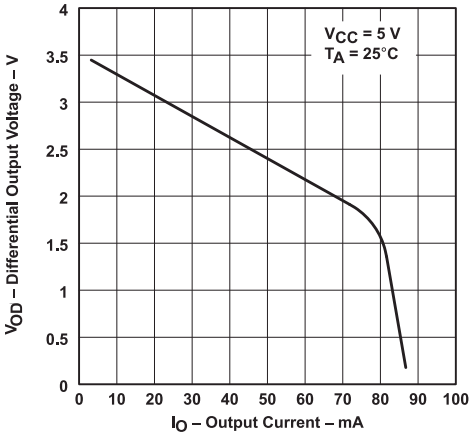



**Figure 3. Driver, Differential Output Voltage vs Output Current**

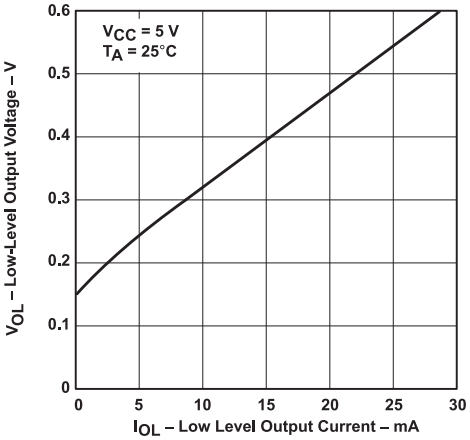



**Figure 4. Receiver, Low-Level Output Voltage vs Low-Level Output Current**

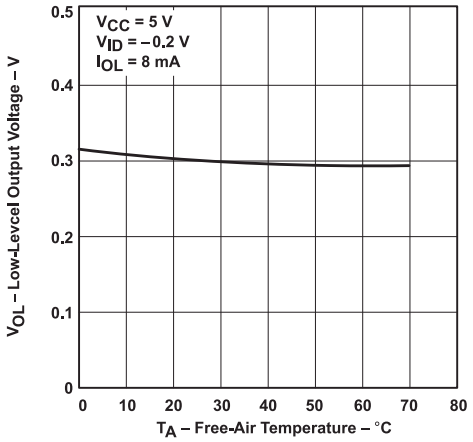



**Figure 5. Receiver, Low-Level Output Voltage vs Low-Level Output Current**

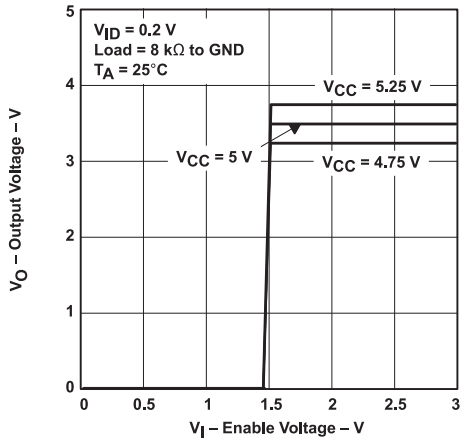



**Figure 6. Low-Level Output Voltage vs Free-Air Temperature**

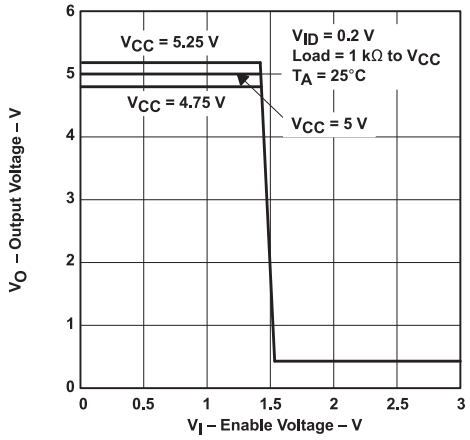



**Figure 7. Output Voltage vs Enable Voltage**

# 7 Parameter Measurement Information

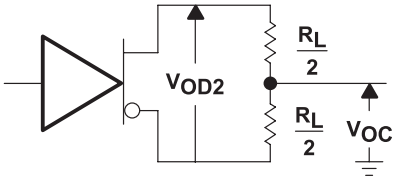



**Figure 8. Driver $V_{OD}$ and $V_{OC}$**

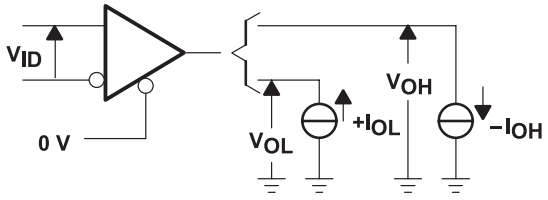
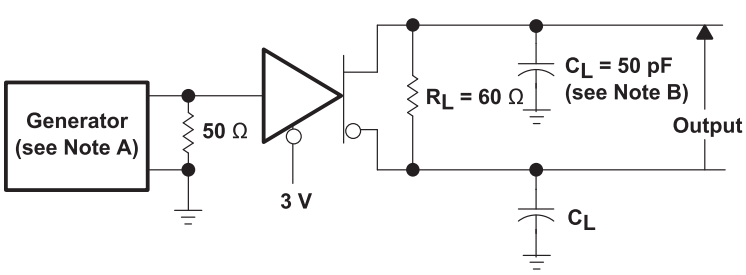
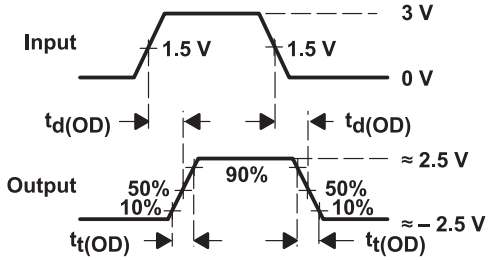



**Figure 9. Receiver $V_{OH}$ and $V_{OL}$**




TEST CIRCUIT

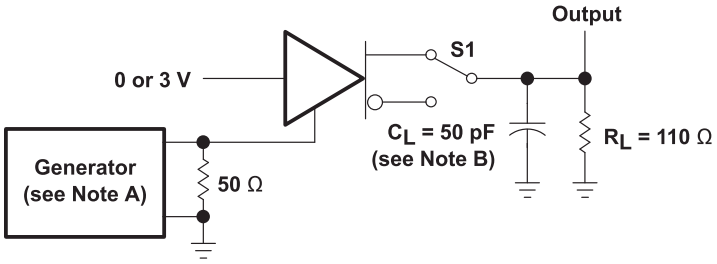



VOLTAGE WAVEFORMS

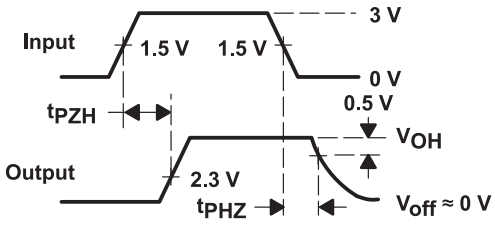
A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 W.

B. $C_L$ includes probe and jig capacitance.

**Figure 10. Driver Test Circuit and Voltage Waveforms**




TEST CIRCUIT

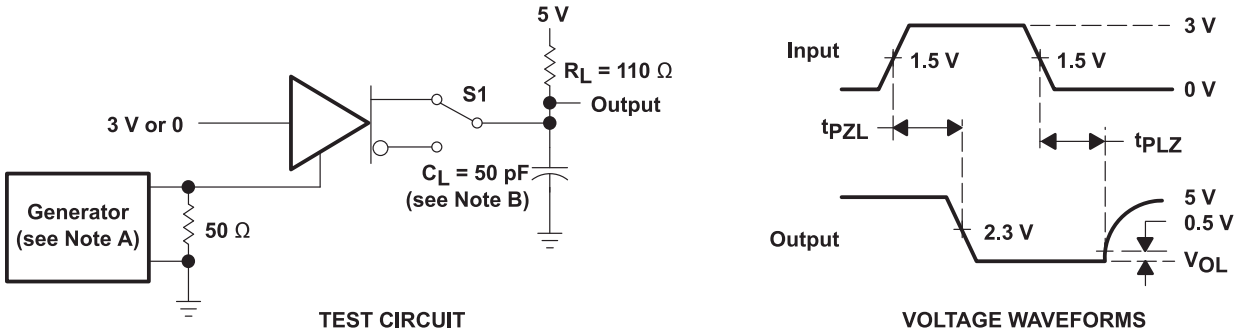



VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 W.

B. $C_L$ includes probe and jig capacitance.

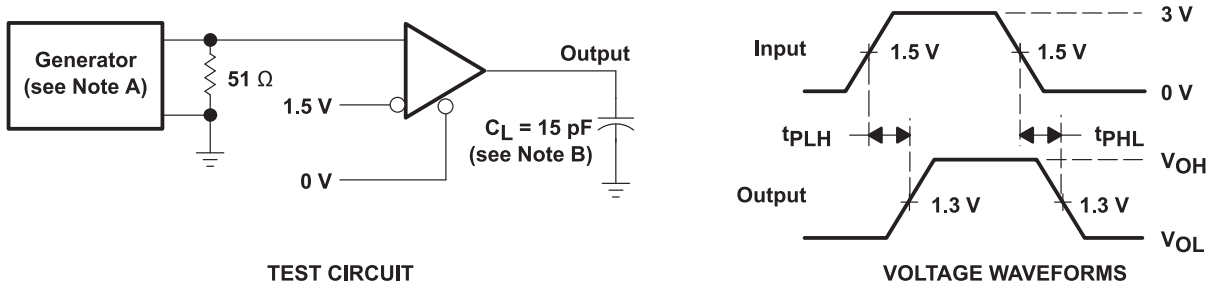
**Figure 11. Driver Test Circuit and Voltage Waveforms**




A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 W.

B. $C_L$ includes probe and jig capacitance.

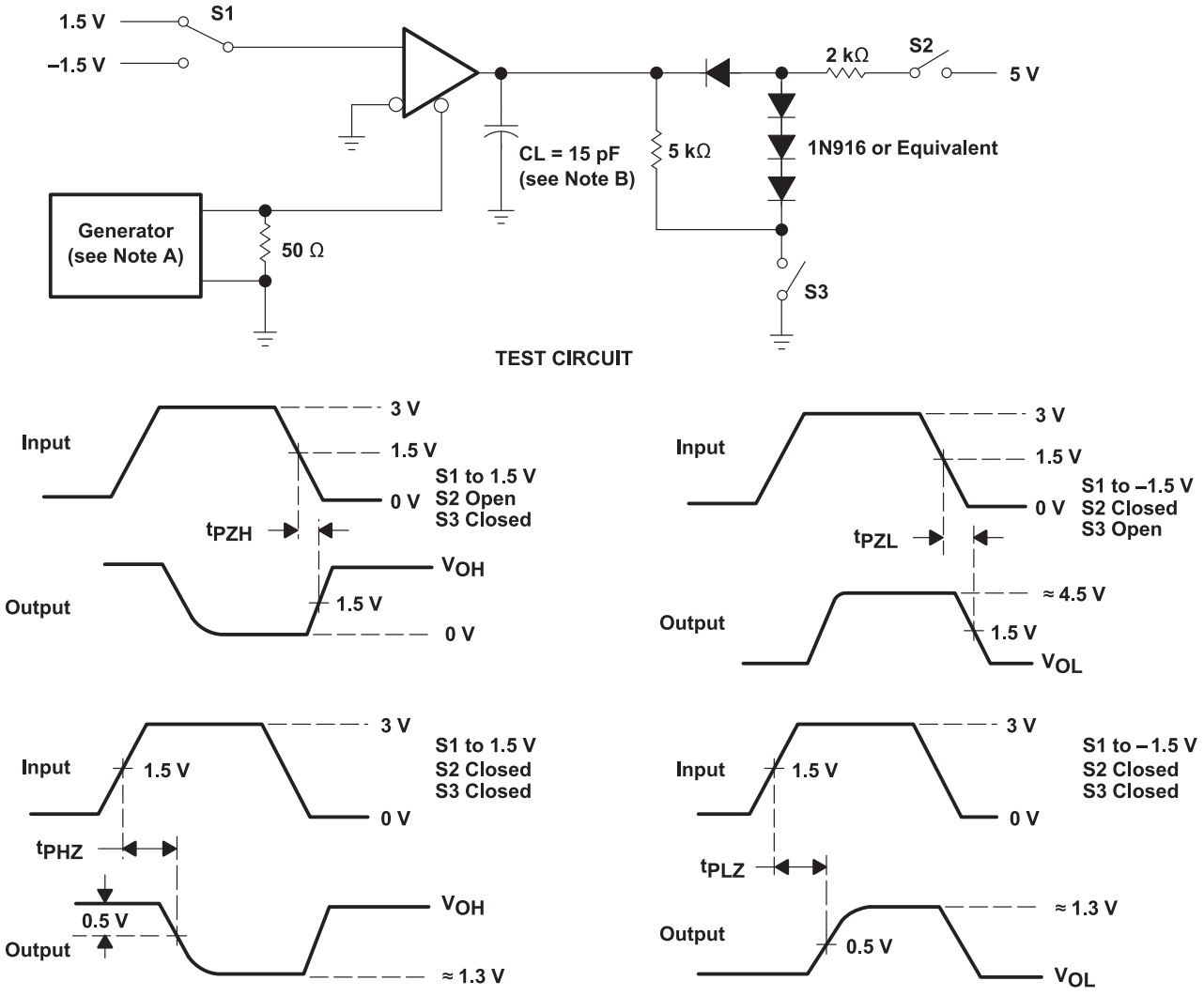
**Figure 12. Driver Test Circuit and Voltage Waveforms**




A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 W.

B. $C_L$ includes probe and jig capacitance.

**Figure 13. Receiver Test Circuit and Voltage Waveforms**




A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r$ ≤ 6 ns, $t_f$ ≤ 6 ns, $Z_O$ = 50 W.

B. $C_L$ includes probe and jig capacitance.

**Figure 14. Receiver Test Circuit and voltage Waveforms**

# 8 Detailed Description

## 8.1 Overview

The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The SN75176A combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or $V_{CC}$ = 0. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

## 8.2 Functional Block Diagrams

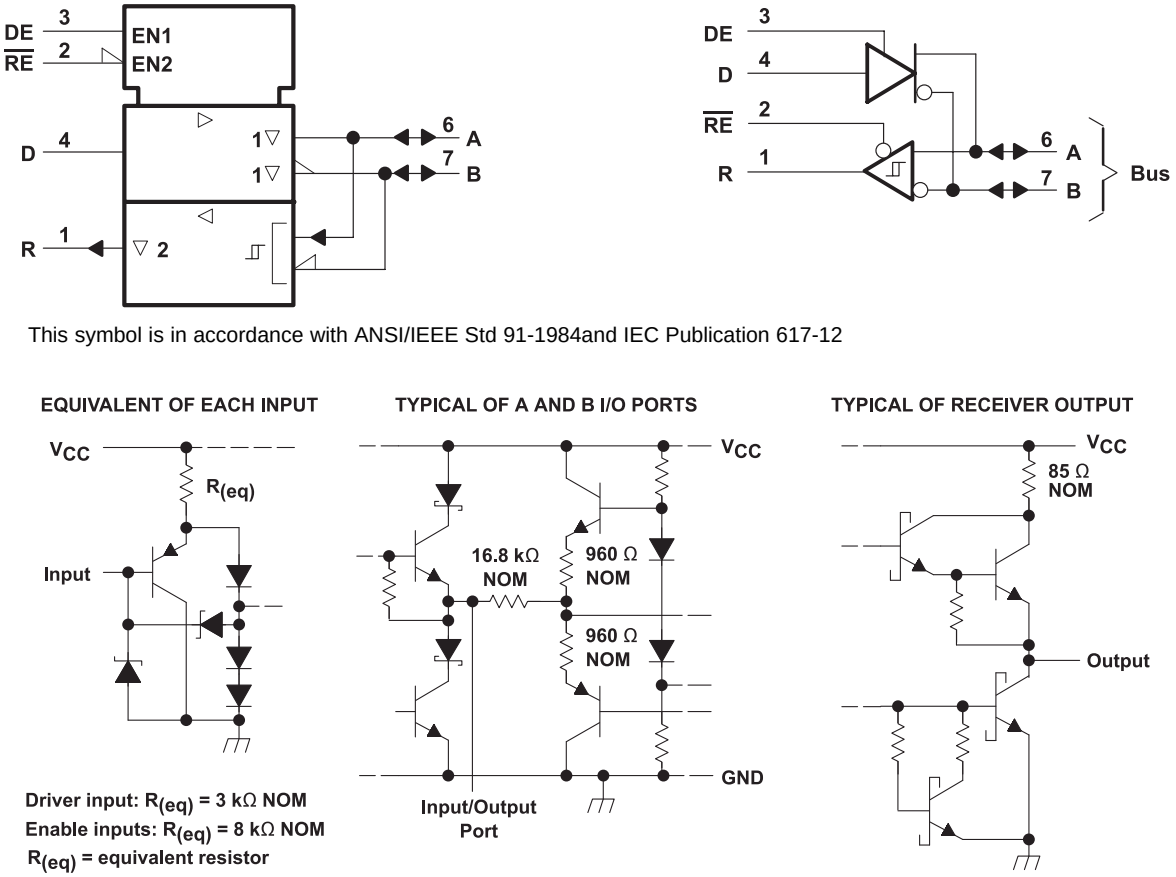



**Figure 15. Schematics of Inputs and Outputs**

## 8.3 Feature Description

### 8.3.1 Driver

The driver converts a TTL logic signal level to RS-422 and RS-485 compliant differential output. The TTL logic input, DE pin, can be used to turn the driver on and off.

**Table 2. Driver Function Table(1)**

| INPUT D | ENABLE DE | DIFFERENTIAL OUTPUTS | |
|---|---|---|---|
| | | A | B |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

(1) H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

### 8.3.2 Receiver

The receiver converts a RS-422 or RS-485 differential input voltage to a TTL logic level output. The TTL logic input, $\overline{RE}$ pin, can be used to turn the receiver logic output on and off.

**Table 3. Receiver Function Table(1)**

| DIFFERENTIAL INPUTS A–B | ENABLE $\overline{RE}$ | OUTPUT R |
|---|---|---|
| $V_{ID} \geq 0.2$ V | L | H |
| $-0.2$ V $< V_{ID} < 0.2$ V | L | U |
| $V_{ID} \leq -0.2$ V | L | L |
| X | H | Z |
| Open | L | U |

(1) H = high level,
L = low level,
U = unkown,
Z = high impedance (off)

## 8.4 Device Functional Modes

### 8.4.1 Device Powered

Both the driver and receiver can be individually enabled or disabled in any combination. DE and $\overline{RE}$ can be connected together for a single port direction control bit.

### 8.4.2 Device Unpowered

The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$.

# 9 Application and Implementation

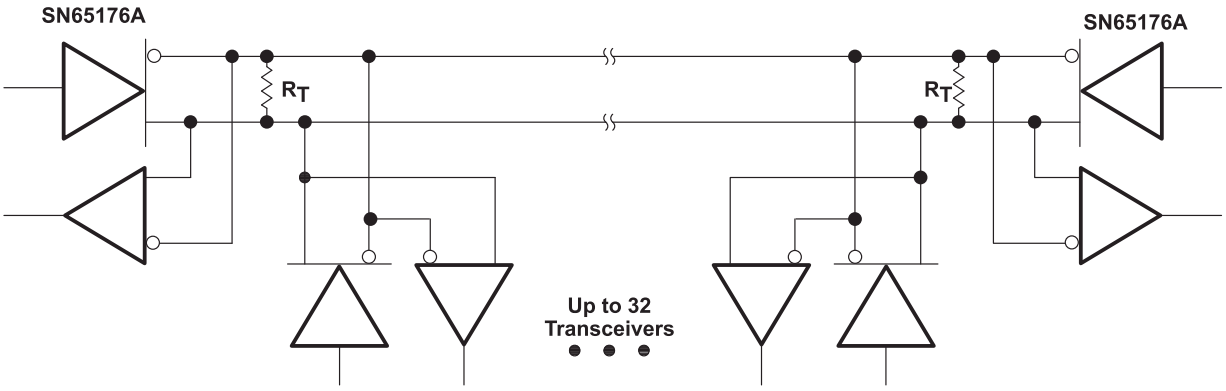
**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

The device can be used in RS-485 and RS-422 physical layer communications.

## 9.2 Typical Application




The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

**Figure 16. Typical Application Circuit**

### 9.2.1 Design Requirements

- 5-V power source
- RS-485 bus operating at 5 Mbps or less
- Connector that ensures the correct polarity for port pins
- External fail safe implementation

### 9.2.2 Detailed Design Procedure

- Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line
- If desired, add external fail-safe biasing to ensure +200 mV on the A-B port.

## Typical Application (continued)

### 9.2.3 Application Curves

A. Scale is 1V per division and 50nS per division

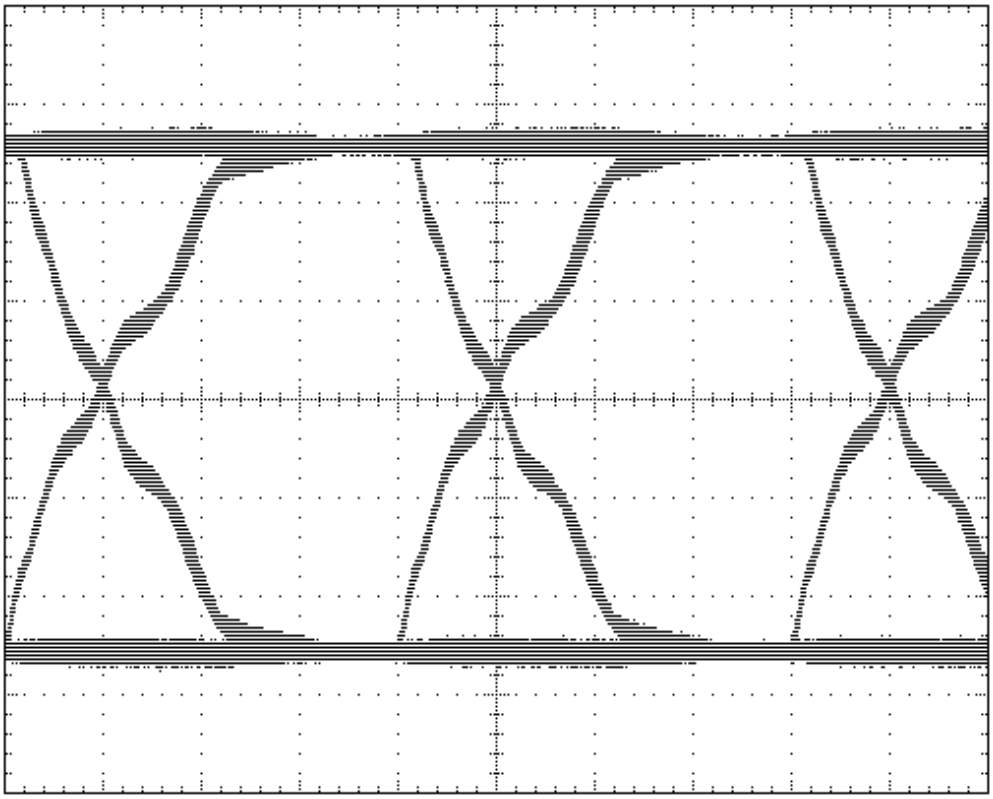


**Figure 17. Eye Diagram for 5-Mbps Over 100 feet of Standard CAT-5E cable 120-Ω Termination at Both Ends.**

## 10 Power Supply Recommendations

Power supply should be 5 V with a tolerance less than 10%

# 11 Layout

## 11.1 Layout Guidelines

Traces from device pins A and B to connector must be short and capable of 250 mA maximum current.

## 11.2 Layout Example

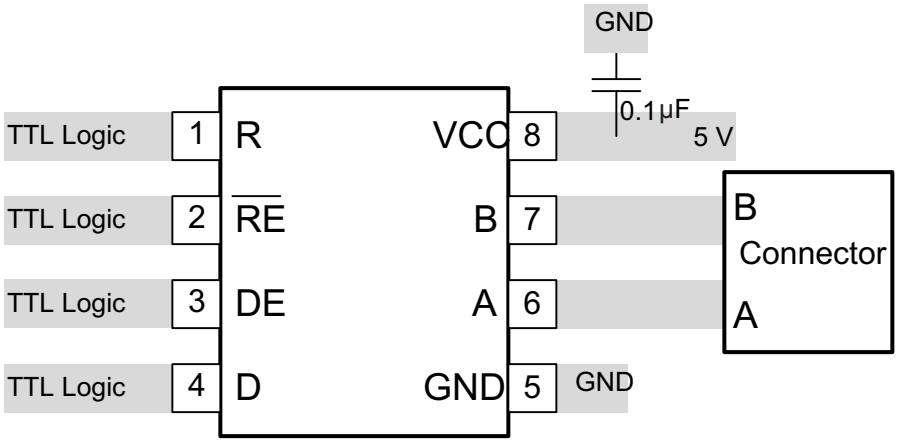



**Figure 18. Layout Example**

# 12 Device and Documentation Support

## 12.1 Trademarks

All trademarks are the property of their respective owners.

## 12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75176AD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75176A | Samples |
| SN75176ADE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75176A | Samples |
| SN75176ADG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75176A | Samples |
| SN75176ADR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75176A | Samples |
| SN75176ADRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75176A | Samples |
| SN75176ADRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75176A | Samples |
| SN75176AP | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN75176AP | Samples |
| SN75176APE4 | ACTIVE | PDIP | P | 8 | 50 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN75176AP | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

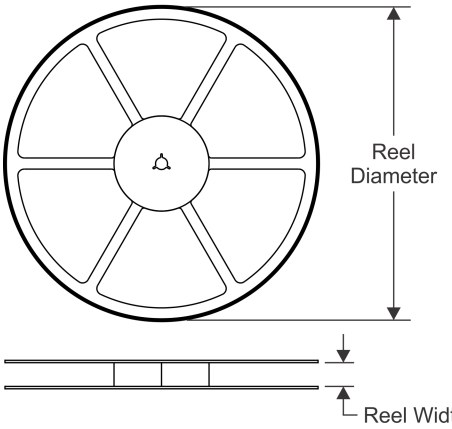
**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

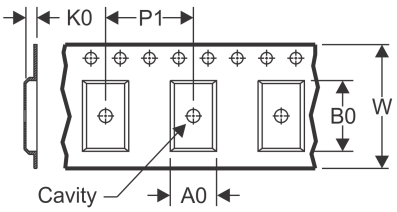
**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

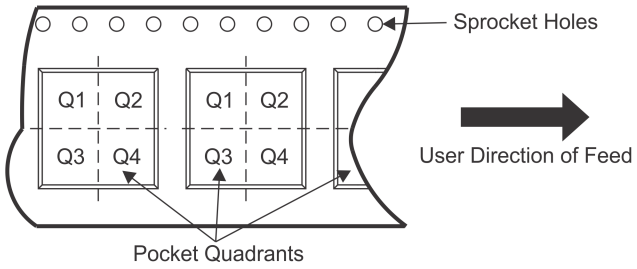



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

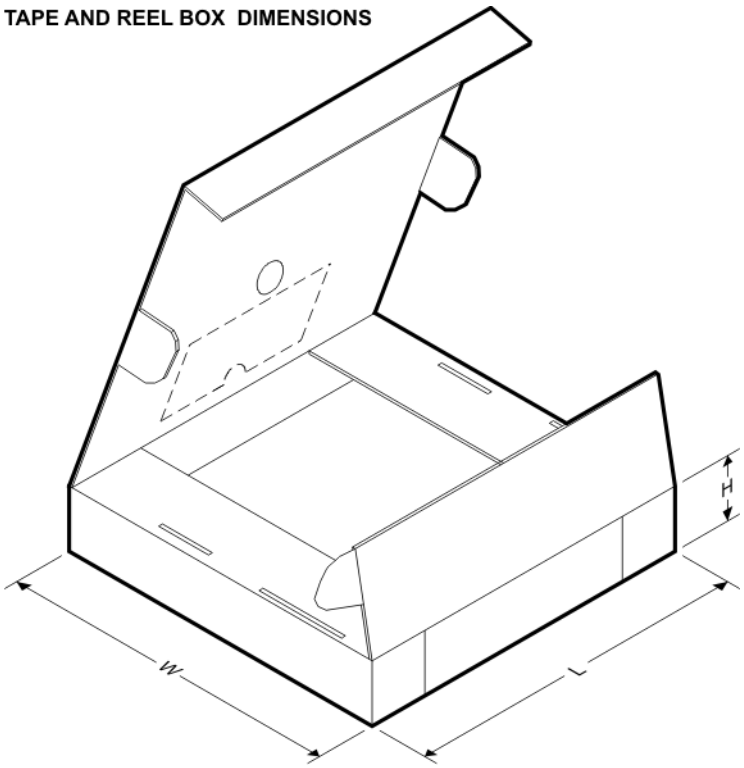
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75176ADR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

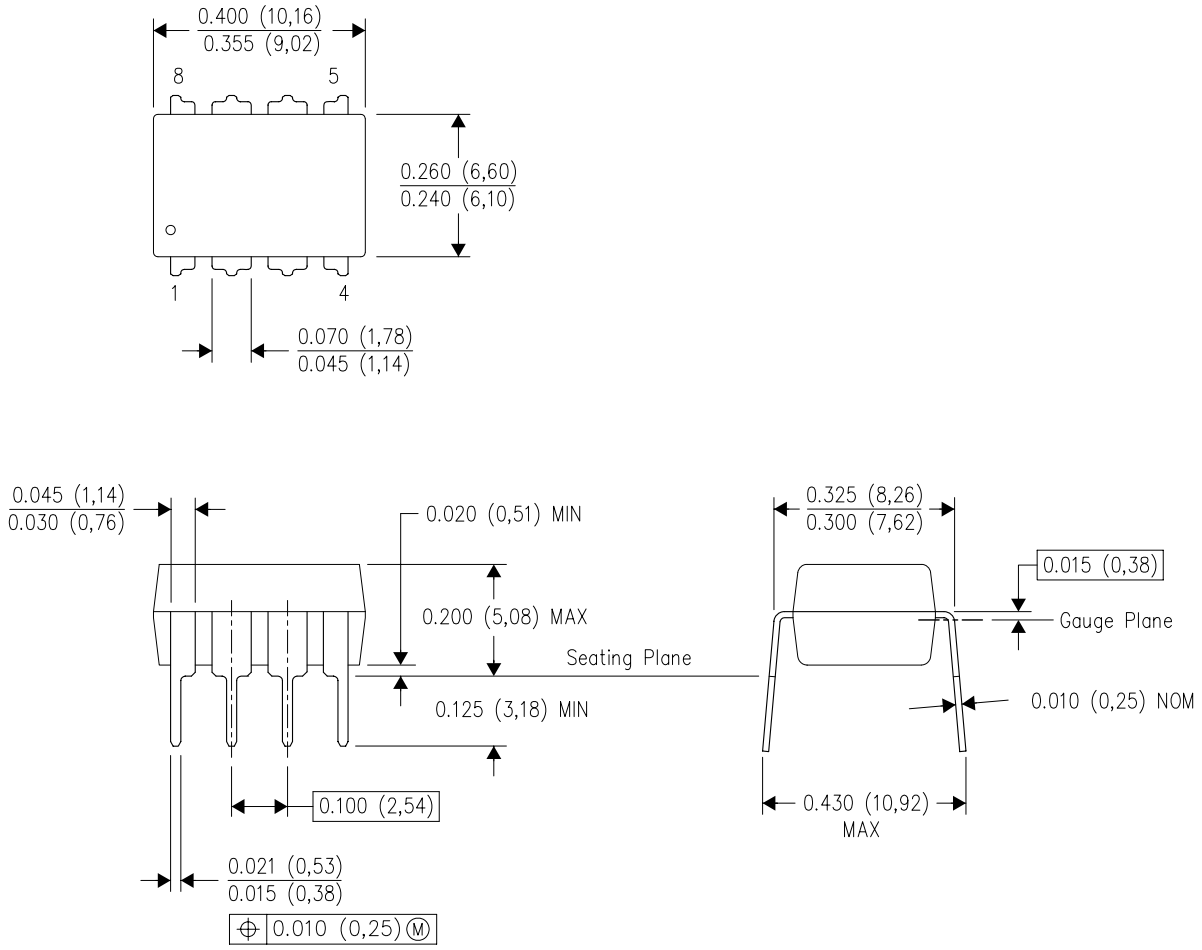
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

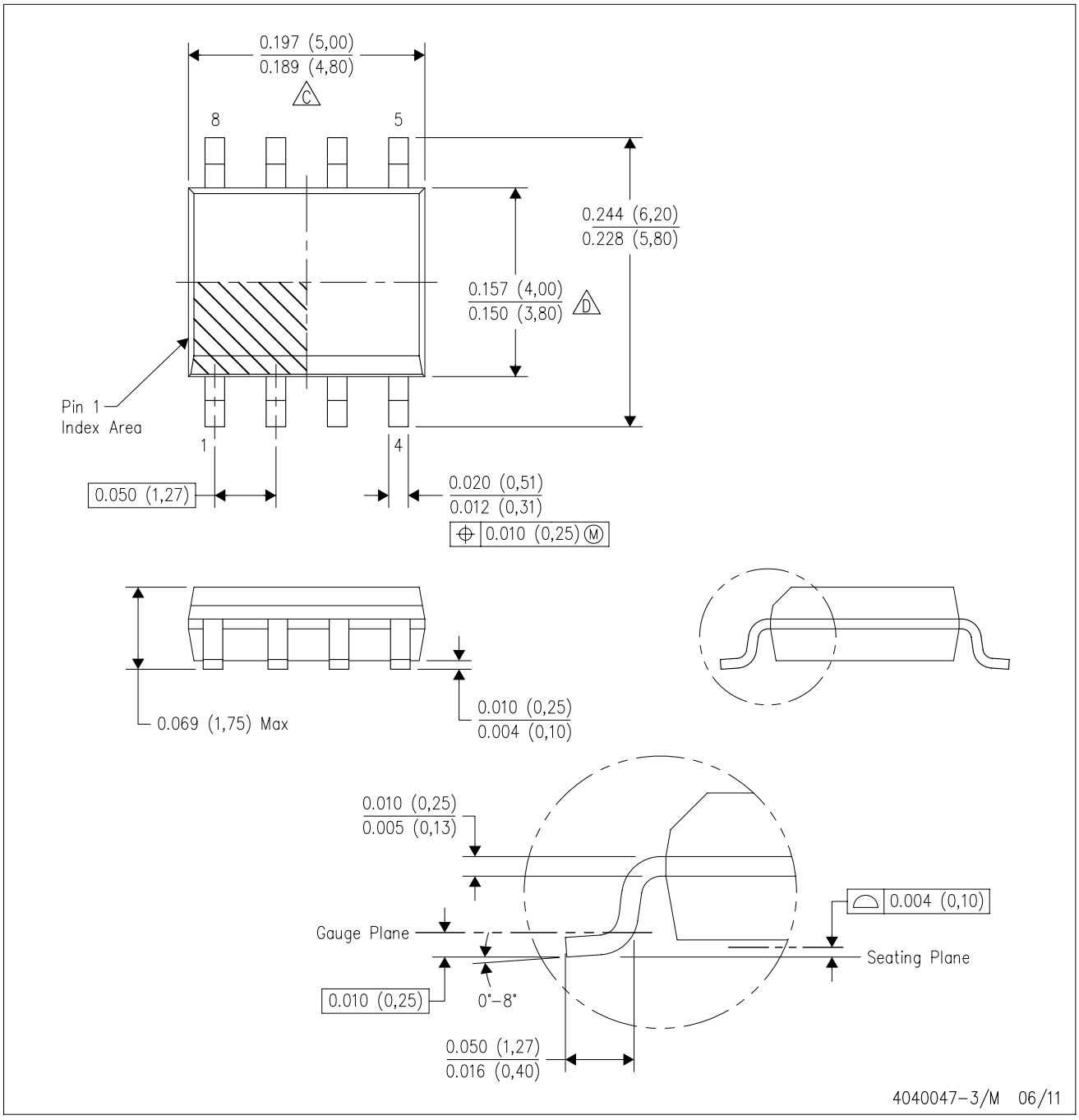
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN75176ADR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



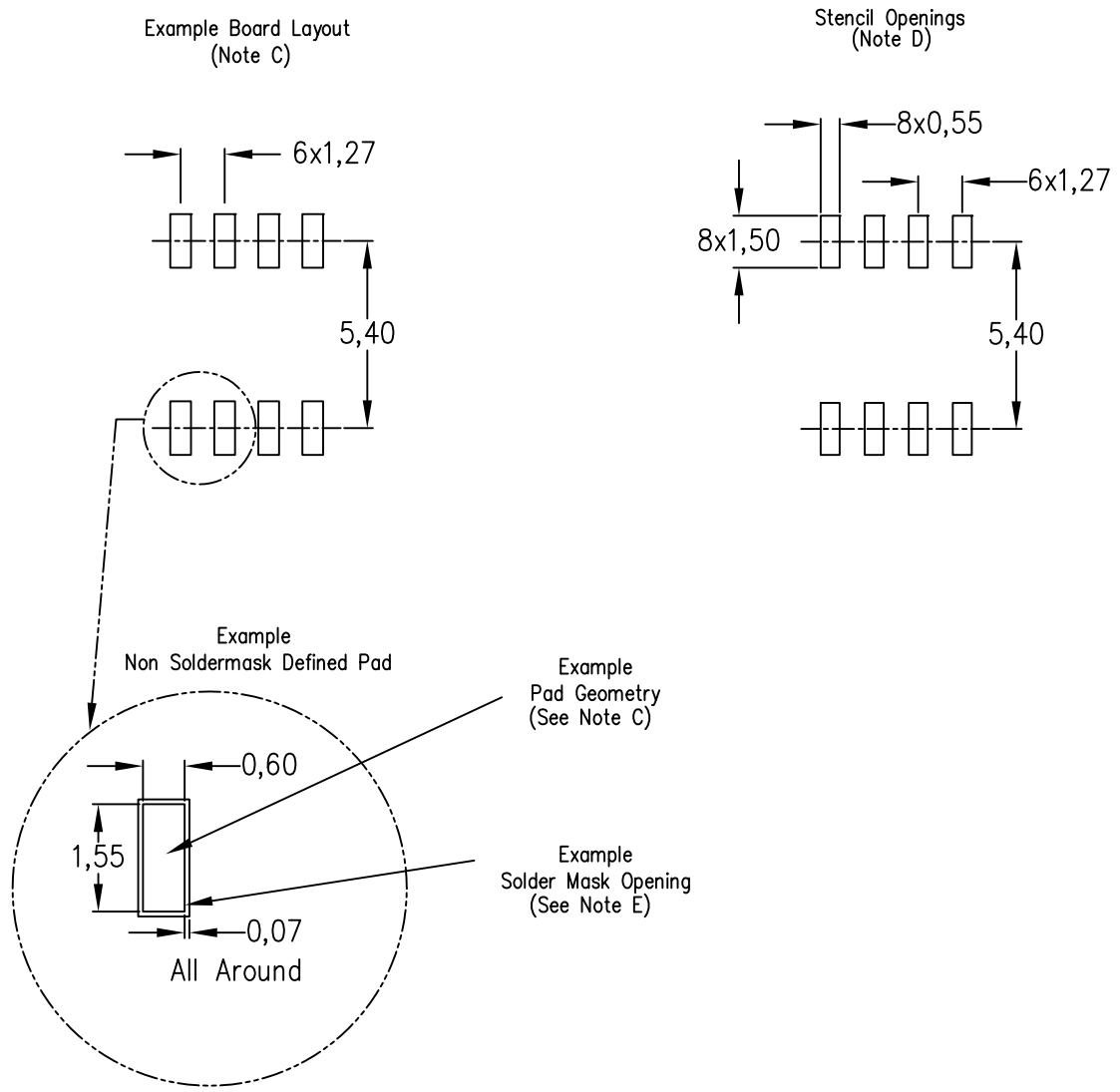

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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