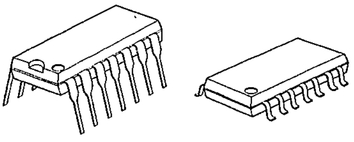
FSK DEMODULATOR/TONE DECODER

■ GENERAL DESCRIPTION

The NJM2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications, and operates over a wide frequency range of 0.01Hz to 300kHz. It can accommodate analog signals between 2mV and 3V, and can interface with conventional DTL, TTL and ECL logic families. The circuit consists of a basic PLL for tracking an input signal frequency within the passband, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set carrier frequency, bandwidth, and output delay.

■ PACKAGE OUTLINE



NJM2211D NJM2211M

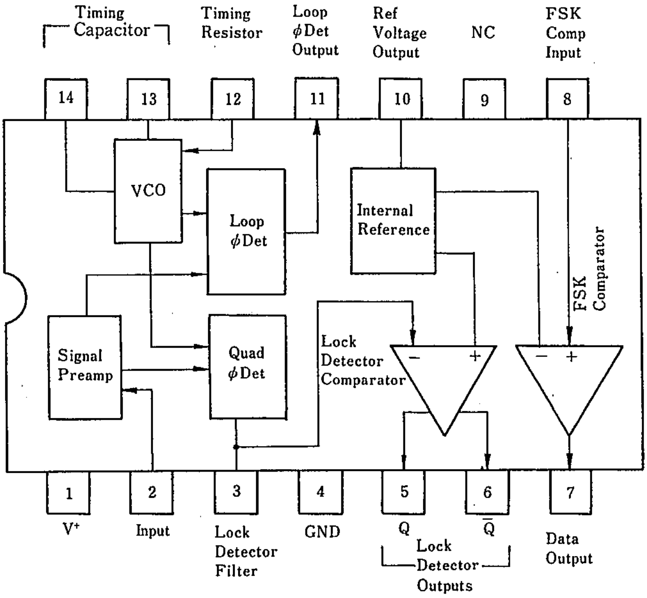
■ FEATURES

- Wide Operating Voltage (4.5V to 20V)
- Wide frequency range (0.01Hz to 300 kHz)
- DTL/TTL/ECL logic compatibility
- FSK demodulation with carrier-detector
- Wide dynamic range (2mV to $3V_{rms}$)
- Adjustable tracking range (±1% to ±80%)
- Excellent temperature stability (20ppm/°C typical)
- Package Outline DIP14, DMP14
- Bipolar Technology

■ APPLICATIONS

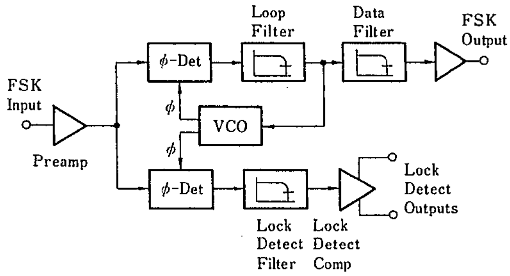
- FSK demodulation
- Data synchronization
- Tone decoding
- FM detection
- Carrier detection

■ PIN CONFIGURATION



NJM2211D
NJM2211M

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	20	V
Input Signal Level	V_{IN}	3	V_{rms}
Power Dissipation	P_D	(DIP14) 700	mW
		(DMP14) 300	mW
Operating Temperature Range	T_{opr}	−40～+85	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

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■ ELECTRICAL CHARACTERISTICS

(V^+=+12V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V^+		4.5	—	20	V
Operating Current	I_{CC}	$R_0 \geqq 10k\Omega$	—	5	11	mA
Oscillator						
Frequency Accuracy	Δf_0		—	±1.0	—	%
Frequency Stability Temp. Coefficient	$\Delta f_0/\Delta T$	$R_1=\infty$	—	±20	—	ppm/°C
Power Supply Rejection	PSRR	V^+=12±1V V^+=5±0.5V	—	±0.05 ±0.2	±1.5	%/V %/V
Upper Frequency Limit	$f_{0\,MAX}$	R_0=8.2kΩ, C_0=400pF	—	300	—	kHz
Lowest Operating Frequency	$f_{0\,MIN}$	R_0=2MΩ, C_0=50μF	—	0.01	—	Hz
Timing Resistor						
Timing Resistor	R_0	Operating Range	5	—	2000	kΩ
		Recommended Range	15	—	100	kΩ
Loop Phase Detector						
Peak Output Current	I_0	Meas. at pin 11	±100	±200	±300	μA
Output Offset Current	I_{OS}		—	±2.0	—	μA
Output Impedance	Z_0		—	1.0	—	MΩ
Maximum Voltage Swing	V_{OM}	Ref. to pin 10	±4.0	±5.0	—	V
Quadrature Phase Detector						
Peak Output Current	I_0	Meas. at Pin 3	—	150	—	μA
Output Impedance			—	1.0	—	MΩ
Maximum Voltage Swing			—	11	—	V_{p-p}
Input Preamp						
Input Impedance	R_{IN}	Meas. at Pin 2	—	20	—	kΩ
Input Signal Voltage Required to Cause Limiting	V_{IN}		—	2	—	mV_{rms}

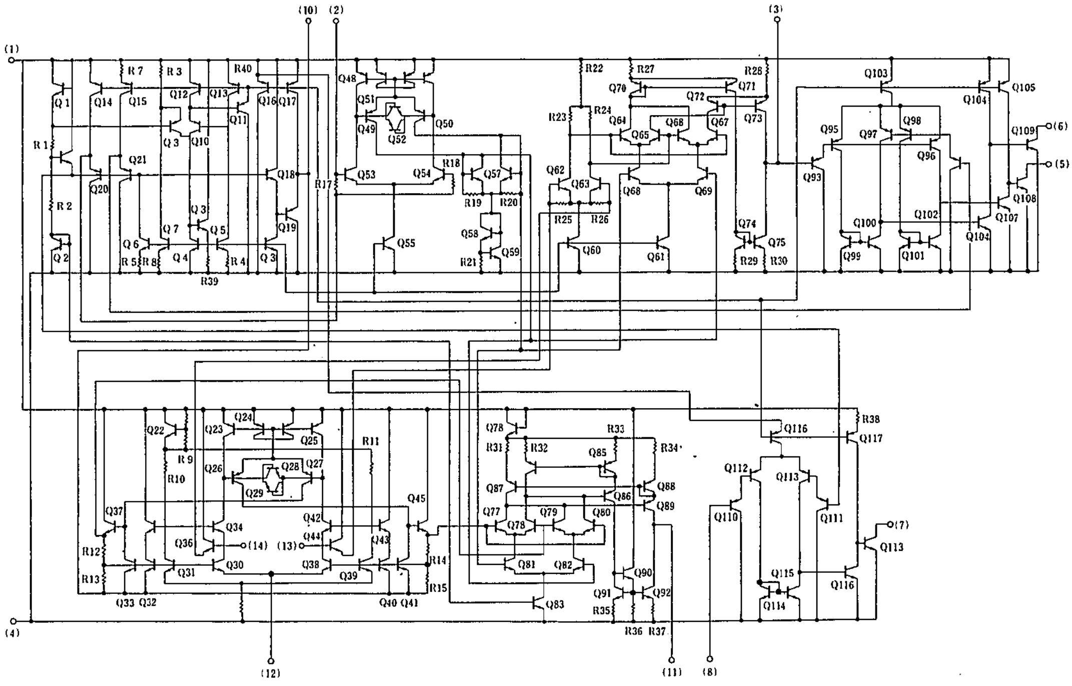
Voltage Comparator

Input Impedance	R_{IN}	Measure at Pin 3 & 8	—	2	—	MΩ
Input Bias Current	I_B		—	100	—	nA
Voltage Gain	G_V	R_L=5.1kΩ	—	70	—	dB
Output Voltage Low	V_{SAT}	5, 6, 7_{PIN} I_C=3mA	—	0.3	1.0	V
Output Leakage Current	I_{LEAK}	V_0=12V	—	0.01	11	μA

Internal Reference

Output Voltage	V_{REF}	Measure at Pin 10	4.75	5.30	5.85	V
Output Impedance	Z_0		—	100	—	Ω

■ EQUIVALENT CIRCUIT



■ CIRCUIT FUNCTION

• Singal Input (Pin 2)

The input signal is AC coupled to this terminal. The internal impedance at pin 2 is 20kΩ. Recommended input signal leveles in the range of $10mV_{rms}$ to $3V_{rms}$.

• Quadrature Phase Detector Output (Pin 3)

This is the high-impedance output of the quadrature phase detector, and is internally connected to the input of lock-detect voltage comparator. In tone detection applications, pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 1) to eliminate chatter at the lock-detect outputs. If this tone-detect section is not used, pin 3 can be left open circuited.

• Lock-Detect Output, Q (Pin 5)

The output at pin 5 is at a "high" state when the PLL is out of lock and goes to a "low" or conducting state when the PLL is locked. It is an open collector type output and required a pull-up resistor, R_L, to V^+ for proper operation. In the "low" state it can sink up to 5mA of load current.

• Lock-Detect Complement, Q (Pin 6)

The output at pin 6 is the logic complement of the lock-detect output at pin 5. This output is also an open collector type stage which can sink 5mA of load current in the low or "on" state.

• FSK Data Output (Pin 7)

This output is an open collector logic stage which requres a pull-up resistor, R_L, to V^+ for proper operation. It can sink 5mA of load current. When decoding FSK signals the FSK data output will switch to a "high" or off state for low input frequency, and will switch to a "low" or on state for high input frequency. If no input signal is present, the logic state at pin 7 is indeterminate.

• FSK Comparator Input (Pin 8)

This is the high-impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase-detector output (pin 11). This data filter is formed by R_F and C_F of Figure 1. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at pin 10.

• Reference Voltage, V_R (Pin 10)

This pin is internally biased at the reference voltage level, V_R; V_R=V+/2−650mV. The DC voltage level at this pin forms an internal reference for the voltage levels at pin 3, 8, 11, and 12. Pin 10 must be bypassed to ground with a 0.1μF capacitor.

• Loop Phase Detector Output (Pin 11)

This terminal provides a high impedance output for the loop phase-detector. The PLL loop filter is formed by R1 and C1 connected to pin 11 (see Figure 1). With no input signal, or with no phase error within the PLL, the DC level at pin 11 is very nearly equal to V_{REF}. The peak voltage swing available at the phase detector output is equal to $\pm V_{REF}$.

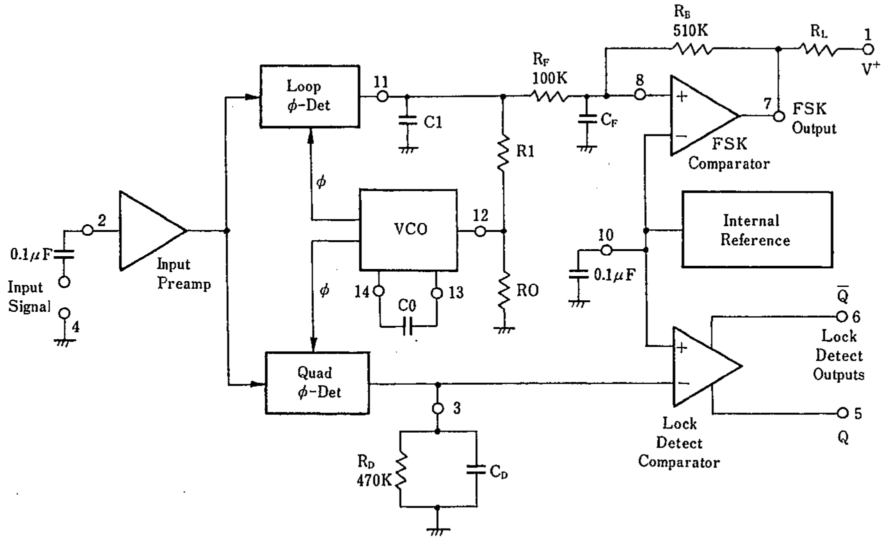


Figure 1 FSK & Tone Detection

• VCO Control Input (Pin 12)

VCO free-running frequency is determined by external timing resistor, R0, connected from this terminal to ground. The VCO free-running frequency, f_0, is given by:

$$f_0(\mathrm{Hz}) = \frac{1}{R0C0}$$

where C0 is the timing capacitor across pins 13 and 14. For optimum temperature stability R0 must be in the range of 10kΩ to 100kΩ (see Typical Electrical Characteristics).

This terminal is a low impedance point, and is internally biased at a DC level equal to V_R. The maximum timing current drawn from pin 12 must be limited to ≦3mA for proper operation of the circuit.

• VCO Timing Capacitor (Pins 13 and 14)

VCO frequency is inversely proportional to the external timing capacitor, C0, connected across these terminals. C0 must be non-polarized, and in the range of 200pF to 10μF.

• VCO Frequncy Adjustment

VCO can be fine tuned by connecting a potentiometer, R_X, in series with R0 at pin 12 (see Figure 2)

• VCO Free-Running Frequency, F_0

The NJM2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase-detector sections of the circuit. However, for setup or adjustment purposes, the VCO free-running frequency can be measured at pin 3 (with C_D disconnected) with no input and also pin 2 shorted to pin 10.

■ DESIGN EQUATIONS

See Figure 1 for Definitions of Components.

1. VCO Center Frequency, f_0:

$$f_0(\mathrm{Hz}) = \frac{1}{R0C0}$$

2. Internal Reference Voltage, V_R (measured at pin 10):

$$V_R = \left(\frac{+V_s}{2}\right) - 650\mathrm{mV}$$

3. Loop Lowpass Filter Time Constant, τ:

$$\tau = R1C1$$

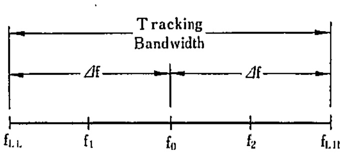
4. Loop Damping, ζ:

$$\zeta = \left(\sqrt{\frac{C0}{C1}}\right)\left(\frac{1}{4}\right)$$

5. Loop Tracking Bandwidth, $\pm\Delta f/f_0$:

$$\Delta f/f_0 = R0/R1$$

$\Delta f/f_0 = R0/R1$



6. FSK Date Filter Time Constant, τ_F:

$$\tau_F = R_F C_F$$

7. Loop Phase Detector Conversion Gain, K_ϕ:

(K_ϕ is the differential DC voltage across pins 10 and 11, per unit of phase error at phase-detector input):

$$K\varphi\ (\text{in volts per radian}) = \frac{(-2)(V_{REF})}{\pi}$$

8. VCO conversion Gain, K0, is the amount of change in VCO frequency per unit of DC voltage change at pin 11:

$$K0\ (\text{in Hertz per volt}) = \frac{-1}{C0R1V_{REF}}$$

9. Total Loop Gain K_T:

$$K_T\ (\text{in radians per second per volt}) = 2\pi K\phi K0 = 4/C0R1$$

10. Peak Phase-Detector Current, I_A:

$$I_A(\mathrm{mA}) = \frac{V_{REF}}{25}$$

■ APPLICATIONS

FSK Decoding

Figure 2 shows the basic circuit connection for FSK decoding. With reference to Figures 1 and 2, the functions of external components are defined as follows: R0 and C0 set the PLL center frequency. R1 sets the system bandwidth, and C1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one pole post-detection filter for the FSK data output. The resistor R_B (=510kΩ) from pin 7 to pin 8 introduces positive feedback across FSK comparator to facilitate rapid transition between output logic states.
Recommended component values for some of the most commonly used FSK bauds are given in Table 1.

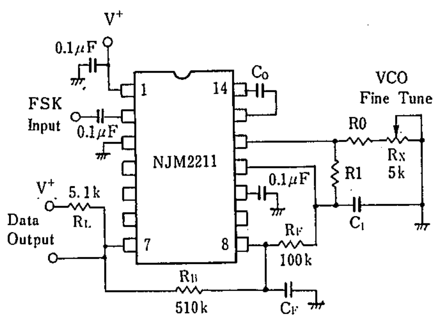


Figure 2 FSK Decoding

Table 1. Recommended Value for FSK
(Ref. Fig. 2)

FSK Band	Component Values
300 Band	C0=0.039μF C_F=0.005μF
F_1=1070Hz	C1=0.01μF R0=18kΩ
f_2=1270Hz	R1=100kΩ
300 Band	C0=0.022μF C_F=0.005μF
f_1=2025Hz	C1=0.0047μF R0=18kΩ
f_2=2225Hz	R1=200kΩ
1200 Band	C0=0.027μF C_F=0.0022μF
f_1=1200Hz	C1=0.01μF R0=18kΩ
f_2=2200Hz	R1=30kΩ

Design Instructions

The circuit of Figure 2 can be tailored for any FSK decoding application by the choice of five key circuit components; R0, R1, C0, C1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

1. Calculate PLL center frequency, f_0
   $$f_0=\frac{f_1+f_2}{2}$$

2. Choose a value of timing resistor R0 to be in the range of 10kΩ to 100kΩ. This choice is arbitary. The recommended value is R0≅20kΩ. The final value of R0 is normally fine-tuned with the series potentiometer, R_X.

3. Calculate value of C0 from Design Equation No. 1 or from Typical Performance Characteristics:
   $C0=1/R0f_0$

4. Calculate R1 to give a Δf equal to the mark-space deviation:
   $R1=R0[f_0/(f_1-f_2)]$

5. Calculate C1 to set loop damping. (See Design Equation No. 4.)
   Normally, $\zeta \approx 1/2$ is recommended
   Then: $C1=C0/4$ for $\zeta=1/2$

6. Calculate Data Filter Capacitance, C_F:
   For R_F=100kΩ. R_B=510kΩ, the recommended value of C_F is:
   $$C_F\,(\text{in }\mu F)=\frac{3}{\text{Band Rate}}$$

Note: All calculated component values except R0 can be rounded off to the nearest standard value, and R0 can be varied to fine-tune center frequency through a series potentiometer, R_X (see Figure 2).

Design Example

75 Band FSK demodulator with mark/space frequencies of 1110/1170Hz:

Step 1: Calculate f_0:

$f_0=(1110+1170)(1/2)=1140\text{Hz}$

Step 2: Choose $R0=20k\Omega$ ($18k\Omega$ fixed resistor in series with $5k\Omega$ potentiometer)

Step 3: Calculate C0 from V_{CO} Frequency vs. Timing Capacitor: $C0=0.044\mu F$

Step 4: Calculate R1: $R1=R0(1140/60)=380k\Omega$

Step 5: Calculate C1: $C1=C0/4=0.011\mu F$

Note: All values except R0 can be rounded off to nearest standard value.

FSK Decoding With Carrier Detect

The lock-detect section of the NJM2211 can be used as a carrier detect option for FSK decoding. The recommended circuit connection for this application is shown in Figure 3. The open-collector lock-detect output, pin 6, is shorted to the data output (pin 7). Thus, the data output will be disabled at "low" state, until there is a carrier within the detection band of the PLL, and the pin 6 output goes "high" to enable the data output.

The Minimum value of the lock-detect filter capacitance C_D is inversely proportional to the capture range, $\pm\Delta f_c$. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C1. For most applications, $\Delta f_c<\Delta f/2$. For $R_D=470k\Omega$, the approximate minimum value of C_D can be determined by:

C_D (μF)$\geqq$16/capture range in Hz

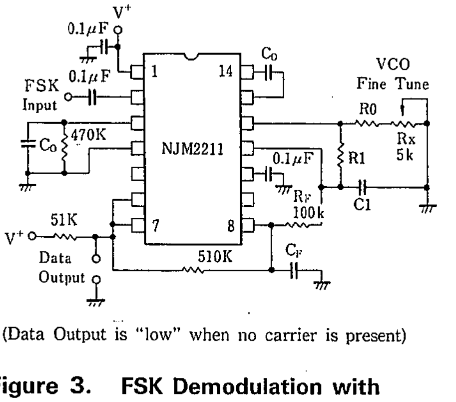
With values of C_D that are too small, chatter can be observed on the lock-detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock-detect output.

Tone Detection

Figure 4 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs becomes reversed for the duration of the input tone. Each logic output can sink 5mA of load current.

Both logic outputs at pins 5 and 6 are open-collector type stages, and require external pull-up resistors R_{L1} and R_{L2} as shown in Figure 4.

With reference to Figure 1 and 4, the function of the external circuit components can be explained as follows: R0 and C0 set VCO center frequency, R1 sets the detection bandwidth, C1 sets the lowpass-loop filter time constant and the loop damping factor, and R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.



(Data Output is "low" when no carrier is present)

Figure 3. FSK Demodulation with Carrier Detect Capability

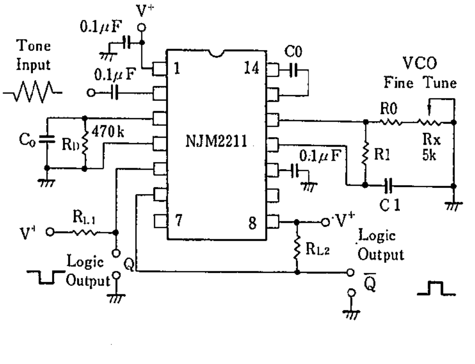


Figure 4. Tone Detection

Design Instructions

The circuit of Figure 4 can be optimized for any tone-detection application by the choice of five key circuit components: R0, R1 C0, C1, and C_D. For a given input tone frequency, f_S, these parameters are calculated as follows:

1. Choose R0 to be in the range of 15kΩ to 100kΩ. This choice is arbitrary.
2. Calculate C0 to set center frequency, f_0 equal to f_S: $C0=1/R0f_S$.
3. Calculate R1 to set bandwidth $\pm\Delta f$ (see Design Equation No. 5): $R1=R0\ (f_0/\Delta f)$

Note: The total detection bandwidth covers the frequency range of $f_0=\Delta f$.

4. Calculate value of C1 for a given loop damping factor:
   $C1=C0/16\zeta^2$
   Normally $\zeta\approx1/2$ is optimum for most tone-detector applications, giving $C1=0.25\ C0$.
   Increasing C1 improves the out-of-band signal rejection, but increases the PLL capture time.
5. Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with $R_D=470k\Omega$, C_D must be:
   $C_D\ (\mu F)\geqq$ (16/capture range in Hz)
   Increasing C_D slows the logic output response time.

Design Examples

Tone detector with a detection band of 1kHz±20Hz:

Step 1: Choose R0=20kΩ (18kΩ in series with 5kΩ potentiometer).
Step 2: Choose C0 for f_0=1kHz: C0=0.05μF.
Step 3: Calculate R1: R1=(R0) (1000/20)=1MΩ.
Step 4: Calculate C1: for $\zeta=1/2$, C1=0.25μF, C0=0.013μF.
Step 5: Calculate C_D: $C_D=16/38=0.42\mu F$.
Step 6: Fine tune the center frequency with the 5kΩ potentiometer, R_X.

4

Linear FM Detection

The NJM2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for the application is shown in Figure 5. The demodulated output is taken from the loop phase detector output (Pin 11), through a post detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 5.

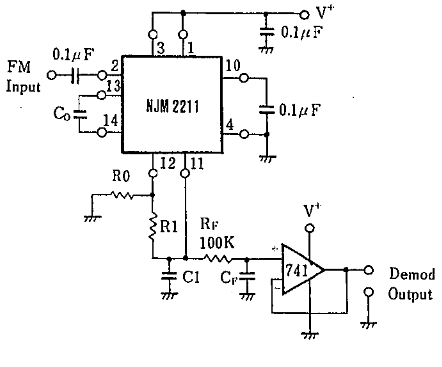


Figure 5. Linear FM Detector

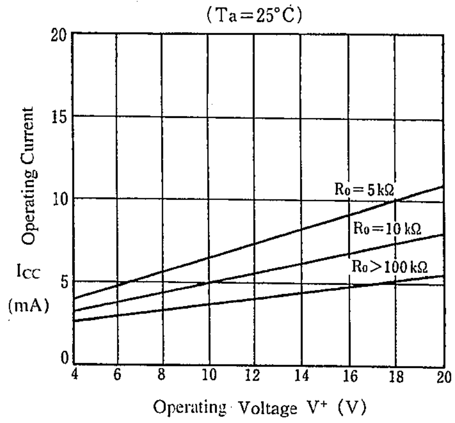
The FM detector gain, i.e., the output voltage change per unit of FM deviation, can be given as:

$V_{OUT}=R1\ V_R/100\ R0$ Volts/% deviation

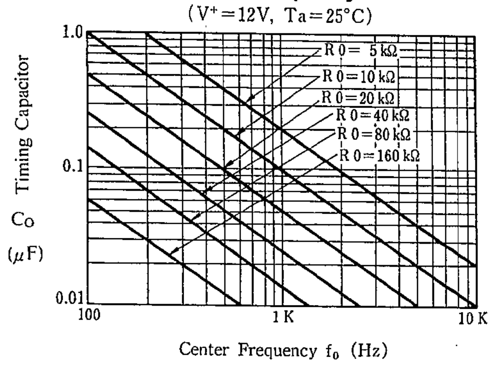
where V_R is the internal reference voltage. For the choice of external components R1, R0, C_D, C1 and C_F, see the section on Design Equations.

■ TYPICAL CHARACTERISTICS

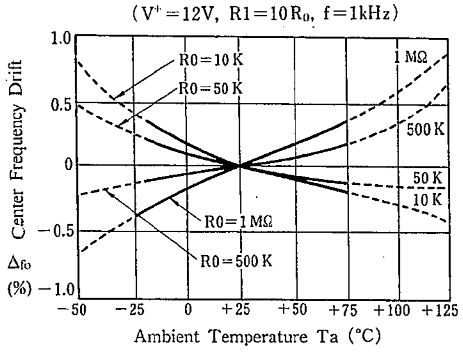
Operating Current
(Ta=25°C)



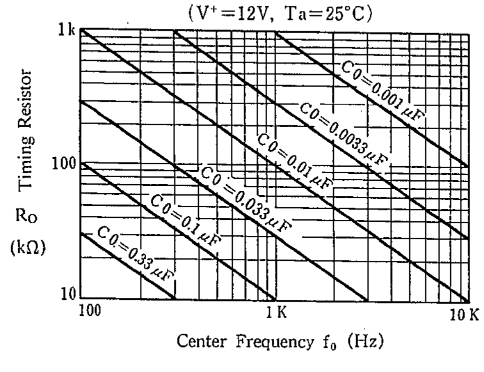
VCO Frequensy
(V+=12V, Ta=25°C)



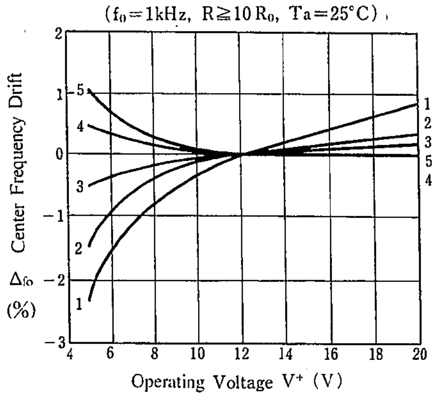
Center Frequency Drift
(V+=12V, R1=10R0, f=1kHz)



VCO Frequency
(V+=12V, Ta=25°C)



Center Frequency
(f0=1kHz, R≧10R0, Ta=25°C)



Curve	R0
1	5 K
2	10 K
3	30 K
4	100 K
5	300 K

MEMO