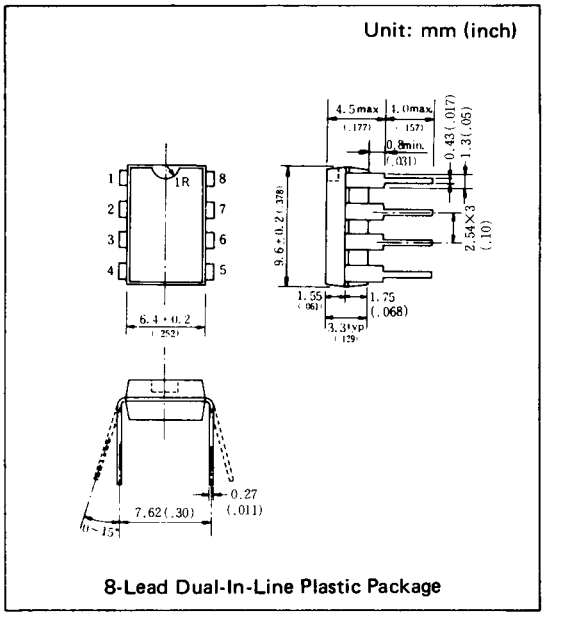
MN3007

1024-STAGE LOW NOISE BBD

■ General description

The MN3007 is a 1024-stage long delay low noise BBD that provides a signal delay of up to 51.2msec.

The MN3007 is particularly suitable for use as reverberation effect of electronic musical instrument such as stereo equipment due to its long delay times.



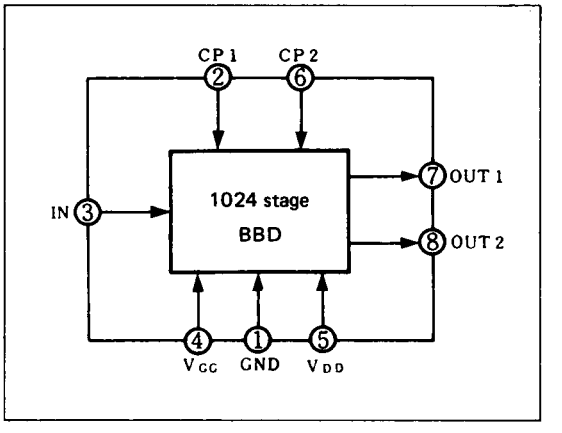
■ Features

- Variable delay time of audio signal: 5.12 ~ 51.2ms.
- Clock component cancellation capability.
- No insertion loss: L_i = 0dB typ.
- Wide dynamic range: S/N ≃ 80dB typ.
- Wide frequency response: $f_i \leqq$ 12KHz.
- Low distortion: THD = 0.5% typ. (V_i = 0.78Vrms).
- Clock frequency range: 10 ~ 100KHz.
- P channel silicon gate process.
- 8-Lead Dual-In-Line Plastic Package.

■ Applications

- Reverberation effect of echo microphone and stereo equipment.
- Chorus effect in electronic musical instrument.
- Variable or fixed delay of analog signals.
- Telephone time compression and delay line for voice communication systems, etc.

■ Block Diagram



■ Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	−15, V_{DD}+1	V
Signal Delay Time	t_D	5.12~51.2	ms
Total Harmonic Distortion	THD	0.5	%
Signal to Noise Ratio	S/N	80	dB

■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−18~+0.3	V
Output Voltage	V_O	−18~+0.3	V
Operating Temperature	Topr	−20~+60	℃
Storage Temperature	Tstg	−55~+125	℃

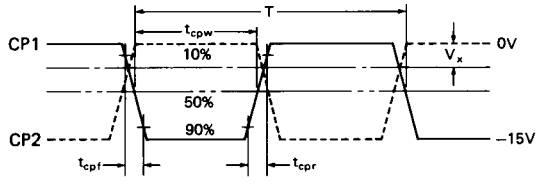
■ Operating Conditions (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}		−14	−15	−16	V
Gate Supply Voltage	V_{GG}			$V_{DD}+1$		V
Clock Voltage "H" Level	V_{CPH}		0		−1	V
Clock Voltage "L" Level	V_{CPL}			V_{DD}		V
Clock Input Capacitance	C_{CP}				700	pF
Clock Frequency	f_{CP}		10		100	kHz
Clock Pulse Width *1	t_{cpw}				0.5T *2	
Clock Rise Time *1	t_{cpr}				500	ns
Clock Fall Time *1	t_{cpf}				500	ns
Clock Cross Point *1	V_X		0		−3	V
Input DC Bias	V_{Bias}		−5		−10	V

■ Electrical Characteristics (Ta = 25°C, $V_{DD} = V_{CPL} = -15V$, $V_{CPH} = 0V$, $V_{GG} = -14V$, $R_L = 100k\Omega$)

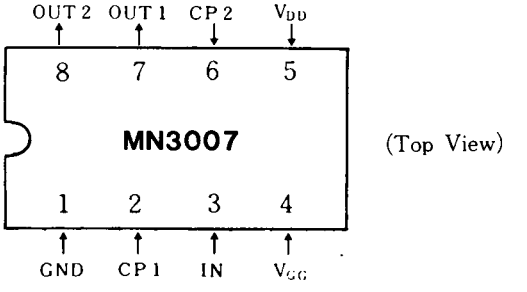
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		5.12		51.2	ms
Input Signal Frequency	f_i	f_{cp} = 40kHz, V_i = 1.5Vrms, 3dB down (0dB at f_i = 1kHz)	12			kHz
Input Signal Swing	V_i	f_{CP}=40kHz, f_i = 1 kHz, THD=2.5%	1.5			Vrms
Insertion Loss	L_i	f_{CP}=40kHz, f_i = 1 kHz, V_i =1.5Vrms	−4	0	4	dB
Total Hamonic Distortion	THD	f_{CP}=40kHz, f_i = 1 kHz, V_i =0.78Vrms		0.5	2.5	%
Noise Voltage	V_{no}	f_{cp} = 100kHz Weighted by "A" curve			0.3	mVrms
Signal to Noise Ratio	S/N			80		dB

*1 Clock Pulse Waveforms



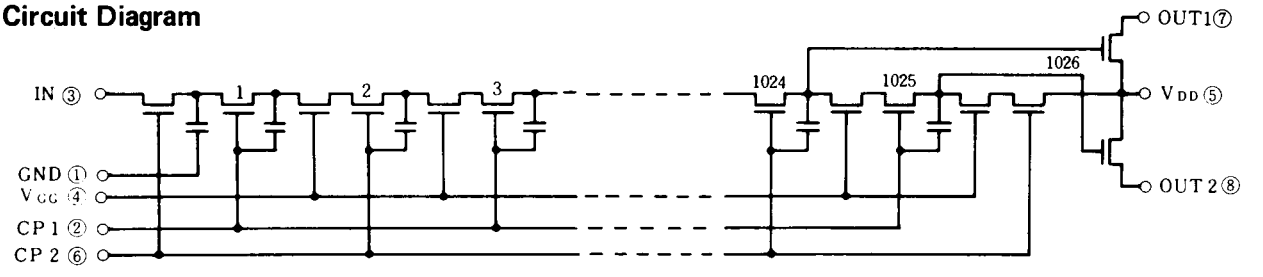
*2 T = $1/f_{CP}$ (Clock period)

■ Terminal Assignments



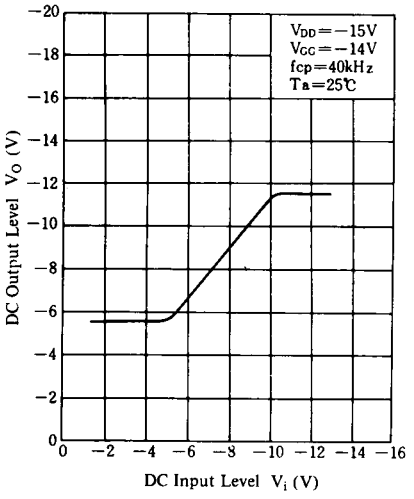
(Top View)

■ Circuit Diagram

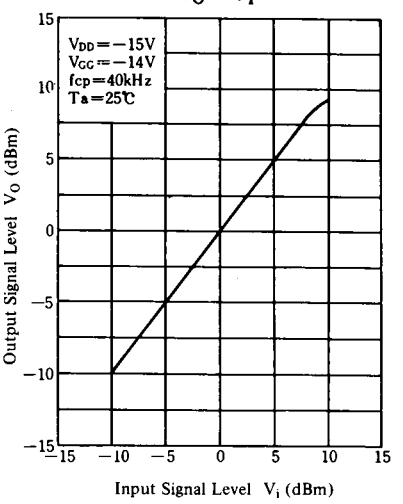


■ Typical Electrical Characteristic Curves

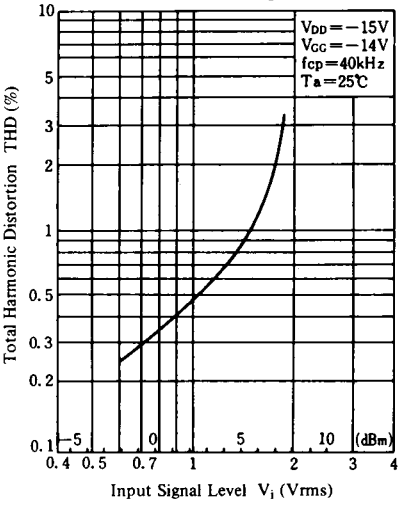
V_O—V_I



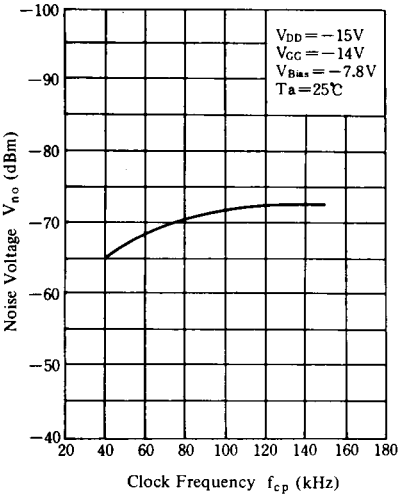
V_O—V_i



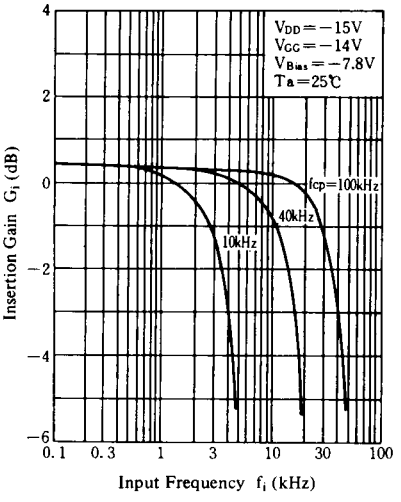
THD—V_i



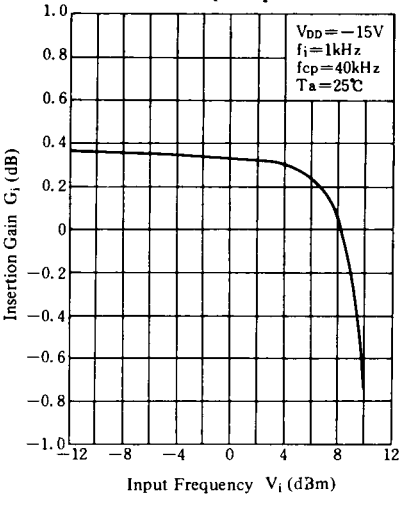
V_{no}—fcp



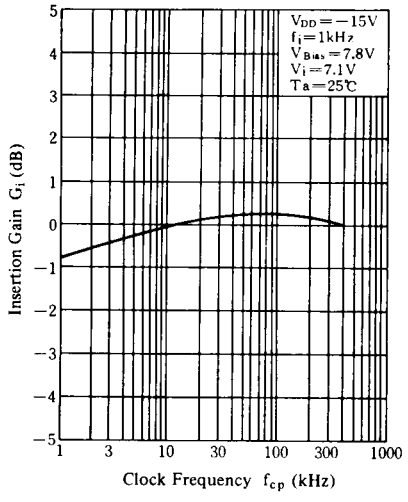
G_i—f_i



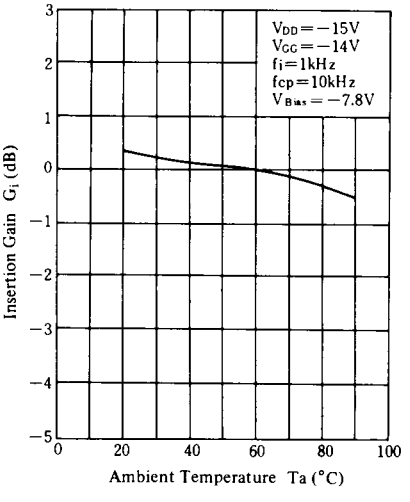
G_i—V_i



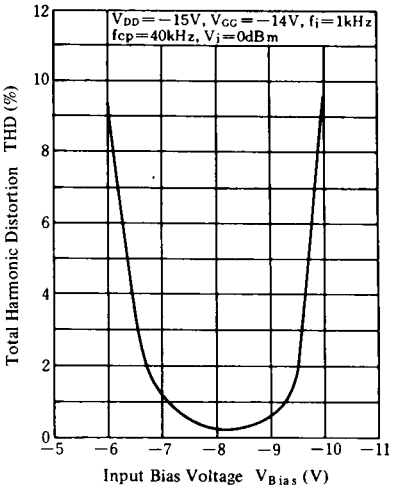
G_i—fcp



G_i—Ta

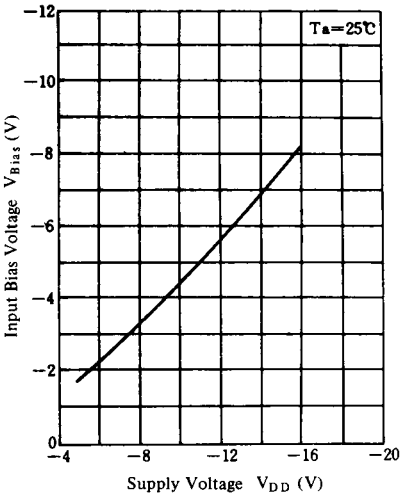


THD—V_{Bias}

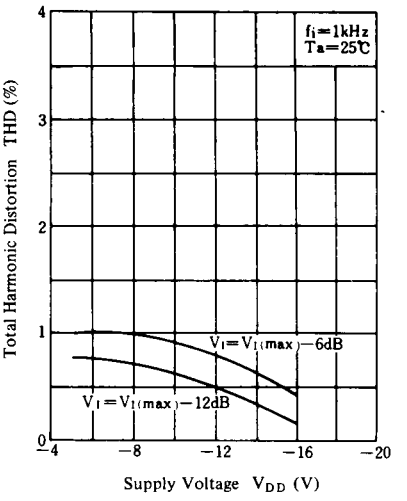


■ Supply Voltage Characteristics

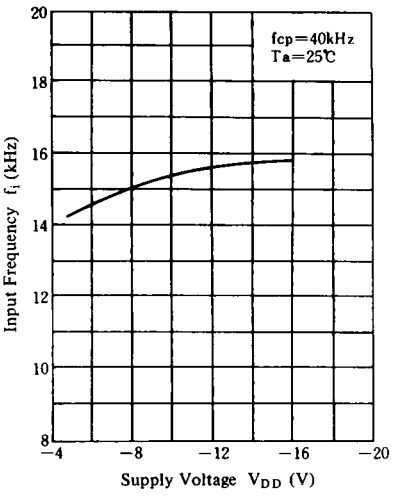
V_{Bias}—V_{DD}



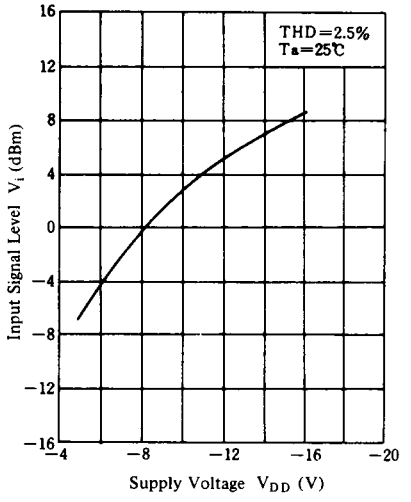
THD—V_{DD}



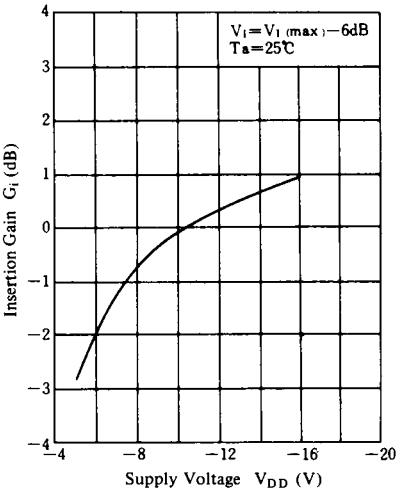
f_i—V_{DD}



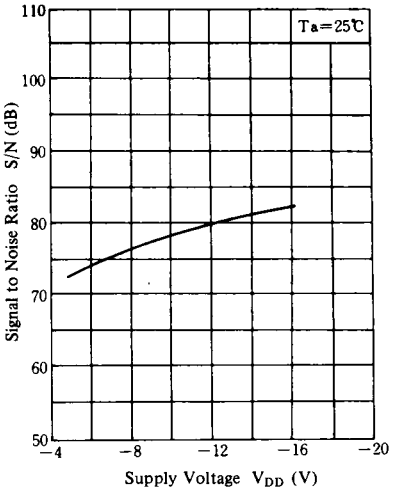
V_i—V_{DD}



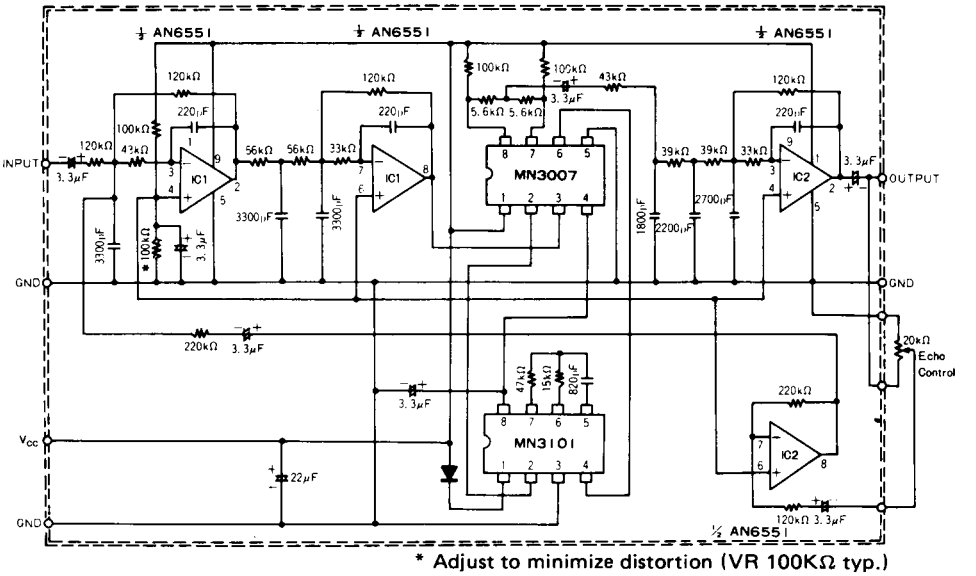
G_i—V_{DD}



S/N—V_{DD}



■ Application Circuit



* Adjust to minimize distortion (VR 100KΩ typ.)

Echo Effect Generation Circuit (Signal Delay Over 10msec.)