MCM2814

Advance Information

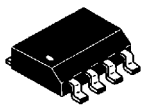
256 x 8 Bit Serial EEPROM

The MCM2814 is a 2048-bit serial electrically erasable PROM designed for handling data in applications requiring both non-volatile memory and in-system information updates.

The MCM2814 is fabricated in 8-pin DIP and SOG packages using floating-gate HCMOS EEPROM technology.

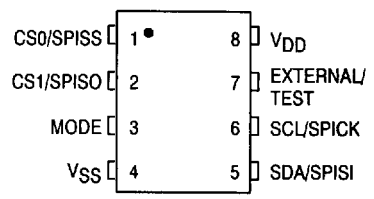
- 2048 Bits Organized as 256 Bytes
- Byte Programmable
- 3 V – 6 V Supply During Read Operations
- On-Chip Programming Voltage Generator
- Two Programming Modes: Two-Wire Serial Access, M-Bus/Four-Wire Serial Access SPI
- Data Protection of 1/4, 1/2, or 3/4 Array with EEPROM Bits
- Simultaneous Programming of 1 to 4 Bytes
- Automatic Byte Address Increment in Read Mode
- Chip Selection with Separate Pin
- Single 3 V to 6 V Supply During Programming
- Digital Filtering on Clock and Data Inputs
- Bit Program Operation: No Byte Erase Necessary
- Data Protection After Reset
- Write/Erase Endurance: 10,000 Cycles over 0 to 70°C
- Typically 100,000 W/E Cycles at Ambient Temperatures
- Data Retention: 10 Years

BP SUFFIX
PLASTIC PACKAGE
CASE 626-04



G SUFFIX
PLASTIC PACKAGE
CASE 751-03

PIN ASSIGNMENT



PIN NAMES

V_{DD}	Power Supply
V_{SS}	Ground (Ref)
External/Test	Connected to On-Chip Voltage Multiplier Output

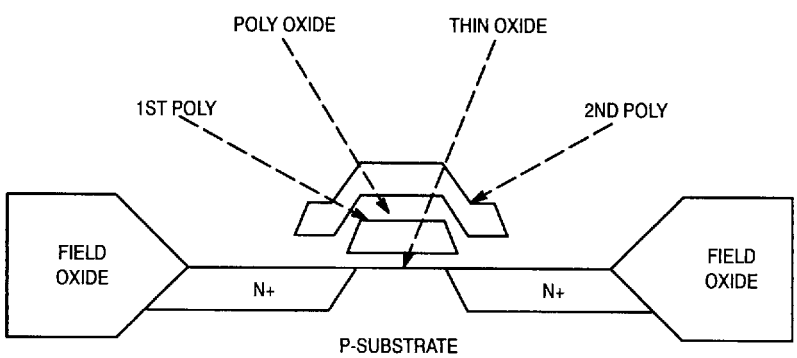
M-BUS MODE

CS0	Chip Select (Hardwired)
CS1	Chip Select (Hardwired)
SDA	Serial Data I/O
SCL	Serial Clock Input

SPI MODE

SPISS	Slave Select Input
SPISO	Serial Data Output
SPISI	Serial Data Input
SPICK	Serial Clock Input

FETMOS
(Floating-Gate Electron Tunnelling MOS)



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This document contains information on a new product. Specifications and information herein are subject to change without notice.

1. PIN DESCRIPTION

1.1 V_{SS}/V_{DD} (Pins 4/8)

V_{DD} and V_{SS} are used to power the circuit. In read mode this supply voltage must be comprised in the V_{DDR} range. (See **5.2 Electrical Characteristics**). In program mode this supply range is limited to V_{DDP}.

1.2 EXTERNAL/TEST (Pin 7)

This pin is used for testing the on-chip voltage multiplier that generates the programming voltage required for a program operation, and should be left open for 5 V only operation.

As this on-chip generator has a high impedance, an external supply can be connected to this pin. This also allows to block any inadvertent programming by maintaining this pin at V_{DD}.

1.3 MODE (Pin 3)

This pin is used to select one of two modes of operation: M-bus mode at the low logic level or SPI mode at high level.

This pin is usually hardwired to V_{SS} or V_{DD}. It should only be changed if the circuit is internally in a standby state. This pin is high impedance when V_{DD} is at V_{SS} level.

1.4 CS1/SPISO (Pin 2)

In M-bus mode, this pin is used for selecting multiple identical chips on the same serial bus. The chip address is formed by 5 bits predefined for this chip, followed by 2 additional chip select bits. These last two bits must correspond to the CS1/CS0 code for proper chip selection. Up to four MCM2814s can be connected on the same SCL and SDA lines. (See Figure 4.)

In SPI mode, this pin is a push-pull slave data output (SPISO). It will shift-out byte addresses and data as described in Section 4.

This pin is usually connected to the data input pin of a SPI master (MISO).

This pin can not be pulled higher than 0.5 V above V_{DD}, even if V_{DD} is at V_{SS} level.

1.5 CS0/SPISS (Pin 1)

In M-bus mode, this pin is used in conjunction with CS1 for chip selection. (See above.)

In SPI mode, this pin is a Slave Select input. In this mode the serial access is deselected when the SPISS input is high, and the SPISO data output pin is forced high impedance. Multiple chips using the same SPICK, SPISI, and SPISO lines, can be selected via this pin as described in Figure 10.

After powering up the device, a falling edge of the SPISS line is required to start the SPI serial access.

This pin is high impedance when V_{DD} is at V_{SS} level.

1.6 SCL/SPICK (Pin 6)

The serial clock is supplied on pin SCL/SPICK. This pin is an input only; therefore, the chip can only operate as a slave under the control of a serial bus master.

The clock input rising edge is used to shift in data present on the SDA/SPISI pin, and the falling edge is used to shift out data on the SDA or SPISO pin.

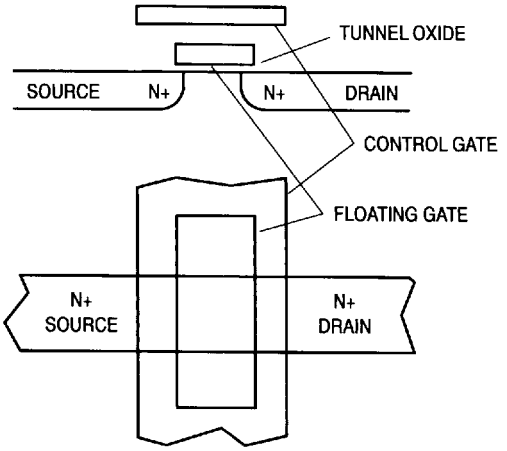
This pin is high impedance when V_{DD} is at V_{SS} level.

1.7 SDA/SPISI (Pin 5)

In M-bus mode, SDA pin is used to transmit data serially in the memory (Receiver) or from the memory (Transmitter). Data transmitted via this pin includes chip addresses, byte addresses, byte data, Read/Write, and acknowledge bits. When SDA is in output, it operates as a pull-down only device (Open-drain). The protocol of this transmission is described in Figures 5 and 6.

In SPI mode, this pin is a Slave data input (SPISI) only and is used to receive opcodes, byte addresses, and byte data. It is usually connected to the data output pin of a SPI master (MOSI).

This pin is high impedance when V_{DD} is at V_{SS} level.



	CG	D	S
READ	0 V	V_{DD}	0 V
PROG 1	0 V	V_{PP}	OPEN
PROG 0	V_{PP}	0 V	0 V

Figure 2. EEPROM Transistor

256 Bytes of EEPROM memory are implemented in a floating gate double poly-silicon process. A Byte Address register is used to select one of the bytes. Three basic states of operation can be distinguished:

- Standby state
- Read state
- Program state

2.1 EEPROM OPERATION

2.1.1 Standby State

In this state, neither a programming, nor a serial transmission occurs, and the power consumption is minimum. (See 3.4.1 and 4.5.)

2.1.2 Read State

In read state, the data of the selected byte is transferred from the memory array to the data shift register used for the serial transmission. This state is active during a serial transmission.

2.1.3 Program State

In this state, a programming voltage higher than V_{DD} is necessary. This voltage is generated by the on-chip voltage multiplier or can be supplied externally. During programming, V_{DD} must be within the V_{DDP} range. (See 5.2)

In M-bus mode, the programming starts at the end of a write command, when a STOP or a new START condition occurs. The programming is enabled at this time, as well as the on-chip voltage multiplier. If there is a capacitive load on the V_{PP} pin, the V_{PP} rise time should be added to the minimum program time t_{PROG}.

In SPI mode, programming could start when a write serial transmission is ended with an SPISS rising edge. Actual programming will happen only if enabled by a V_{PP} enable serial command. This command can be transmitted before or after the write sequence.

2.2 EEPROM DATA PROTECTION

Some circuitry has been included to prevent unwanted modification of EEPROM data, and is described below. However, a noisy serial link is very often the cause of bad data or data written to the wrong address. Besides measures to reduce this noise on the board, the serial clock and data inputs (SCL/SDA) have Schmitt triggers and digital filters to reject some of the noise.

2.2.1 Power Up Reset

Immediately after power is applied, programming is inhibited to prevent EEPROM data loss during the system power up.

In both modes, this condition is removed when a READ is performed.

In M-bus mode, this condition is removed by reading the data in any byte address using the normal read sequence.

In SPI mode, it is sufficient to send the READ opcode before a new V_{PP} enable command and the write sequence.

At Reset the following circuitry is initialized:

- The circuit is in standby state
- In M-bus mode, it is waiting for a start condition
- In SPI mode, it is waiting for a high to low SPISS transition
- The data outputs are high impedance (SDA, SPISO)
- The programming is disabled
- The on-chip V_{PP} generator is off

2.2.2 Programming Voltage Enable

In SPI mode only, an internal programming voltage enable flip-flop can be set or cleared with two separate opcodes, thus reducing the risk of unwanted EEPROM programming.

2.2:3 Array Write Protect

In both modes, byte address 255 ($FF) contains EEPROM bits with a special function. When one or two bits of this address are programmed at once, the programming of EEPROM sections is inhibited according to Table 1.

Table 1. EEPROM Write Protect

Data at ADDR $FF		Protected Addresses	No. of Bytes Protected
XXXX	00XX	No Write Prot.	—
XXXX	01XX	$C0 – $FB	60
XXXX	10XX	$80 – $FB	124
XXXX	11XX	$40 – $FB	188

This protection is reversible as address 255 ($FF) can be modified at any time.

2.3 EEPROM PROPERTIES

NO ERASE: Unlike most EEPROMs, it is not necessary to erase a byte before writing new data.

The program operation takes t_{PROG} and must be externally timed.

CUMULATIVE: As the programming operation is under external control, it can be done at once or at various time frames as long as the total programming time exceeds the specified minimum t_{PROG} value.

t_{PROG} is defined with V_{PP} at its programming level.

SELF LIMITING: Excess programming has no positive effect, as programmed EEPROM thresholds will asymptotically reach their nominal values. Programming durations above the recommended maximum t_{PROG} have negative impacts on the EEPROM programming endurance.

2.4 EEPROM RELIABILITY

Reliability figures are statistical in nature; therefore, no minimum or maximum specifications can be applied. The result of reliability tests will be published instead. These tests are conducted on a regular basis during the production life of a circuit and reports are available upon request.

2.4.1 Data Retention

Typical data retention should exceed 10 years for the specified operating temperature range. Data retention is usually tested with the device under bias, but without accessing the EEPROM array.

2.4.2 Read Stress

Unlike some non-volatile memories, there should be no disturbance of the stored data under continuous read of EEPROM bytes. The life limit under continuous read condition should therefore be similar to the normal operating life of the device.

2.4.3 Program Endurance

As for all EEPROMs, there is a wearout mechanism associated with the programming mechanism on the non-volatile memory. More than 10,000 programming cycles should be possible per memory bit; additionally, 100,000 cycles is typical for the specified temperature range. A programming cycle is defined as a 0 to 1 to 0 programming. Unlike most EEPROMs where the whole byte is erased before being reprogrammed, if just one bit is modified in a byte, only this bit will see the programming stress.

Some endurance experiments have shown that the number of programming cycles can be increased if the V_{PP} rise time is increased. This can be achieved with an external capacitor on V_{PP} when the on-chip V_{PP} generator is used. In SPI mode, the V_{PP} should be enabled after the write command has been transmitted. If an external V_{PP} is provided, it should be ramped up only after the write command is transmitted. In this case, a V_{PP} above the maximum value also has a negative impact on the endurance.

2.5 V_{PP} VOLTAGE MULTIPLIER

In M-bus mode, the on-chip V_{PP} generator is turned on or off automatically during a program sequence.

In SPI mode, it is switched on only after a serial V_{PP} enable command has been issued, independently of write or read commands.

3. M-BUS OPERATING MODE

This MODE pin can be hardwired to V_{DD} or V_{SS} to select two different modes of operation. Differences are at the serial transmission level and in the EEPROM operation. They are called M-bus mode and SPI mode.

3.1 M-BUS MODE

Only two wires are needed to control the device operation. The serial transmission of this mode is similar to the IIC™ serial communication standard. It features:

- Up to 4 identical chips on the same 2 wire bus
- CS1/CS0 pins for chip selection
- SCL clock line, input only
- SDA line used as Input and Output
- Data acknowledge bit generated
- Auto programming after reception of new data
- Programming time under external control
- Write inhibit after reset

3.2 LEXICON

This lexicon will describe some terms used in this serial interface description.

MASTER: The device that initiates the serial transmission is designated as master. In general, it is the device generating the clock. This memory can never function as a master.

SLAVE: This memory always operates as a slave.

TRANSMITTER: The device with its SDA pin in output is a data transmitter. In the case of multiple devices in output, the device sending a low level will win due to the Open-Drain connection.

RECEIVER: A device that has been properly selected by a chip address followed by a write bit is a receiver, and will shift data present on the SDA pin in internal registers.

MSB: The Most Significant Bit is the first bit transmitted and received.

START CONDITION: The start condition is defined as a 1 to 0 transition of SDA when SCL is high. The first byte of data following a start condition includes the chip address followed by the Read/Write bit. All devices connected on the same bus receive this data to check if they are addressed.

STOP CONDITION: The stop condition is defined as a 0 to 1 transition of SDA when SCL is high. In this circuit, the stop condition is never mandatory. An EEPROM programming can be initiated by the STOP or also by any following START condition.

A STOP after a serial read sequence will put the device in standby state.

CHIP ADDRESS: The first byte transmitted after a START contains the chip address followed by the Read/Write bit. The 7 bit chip address is formed of 5 fixed bits followed by 2 chip select bits.

Fixed bits are 1010X for this device (X is a don't care bit). The 2 chip select bits must correspond to the 2 chip select inputs for proper chip selection. By this means, up to 4 identical chips can be connected on the same SDA/SCL lines, in order to form a memory bank of up to 8 KBits.

READ/WRITE BIT: The 8th bit transmitted by the master after the 7 bit chip address will indicate the direction of transfer for the next bytes (until a new start or stop). If low, the following bytes are transmitted by the master. If high, the following bytes are transmitted by the MCM2814.

BYTE ADDRESS: The first byte of data received by the memory after the chip address, will be latched in the byte address register and is used to select one of the 256 EEPROM bytes.

ACKNOWLEDGE BIT: This bit is sent by the selected receiver on the data line after a byte reception. Due to the open drain structure, a valid acknowledge bit corresponds to a low level. While operating as a transmitter, sending a sequence of data bits, this device will check the acknowledge bit generated by the master. The absence of this bit will stop the transmission of data.

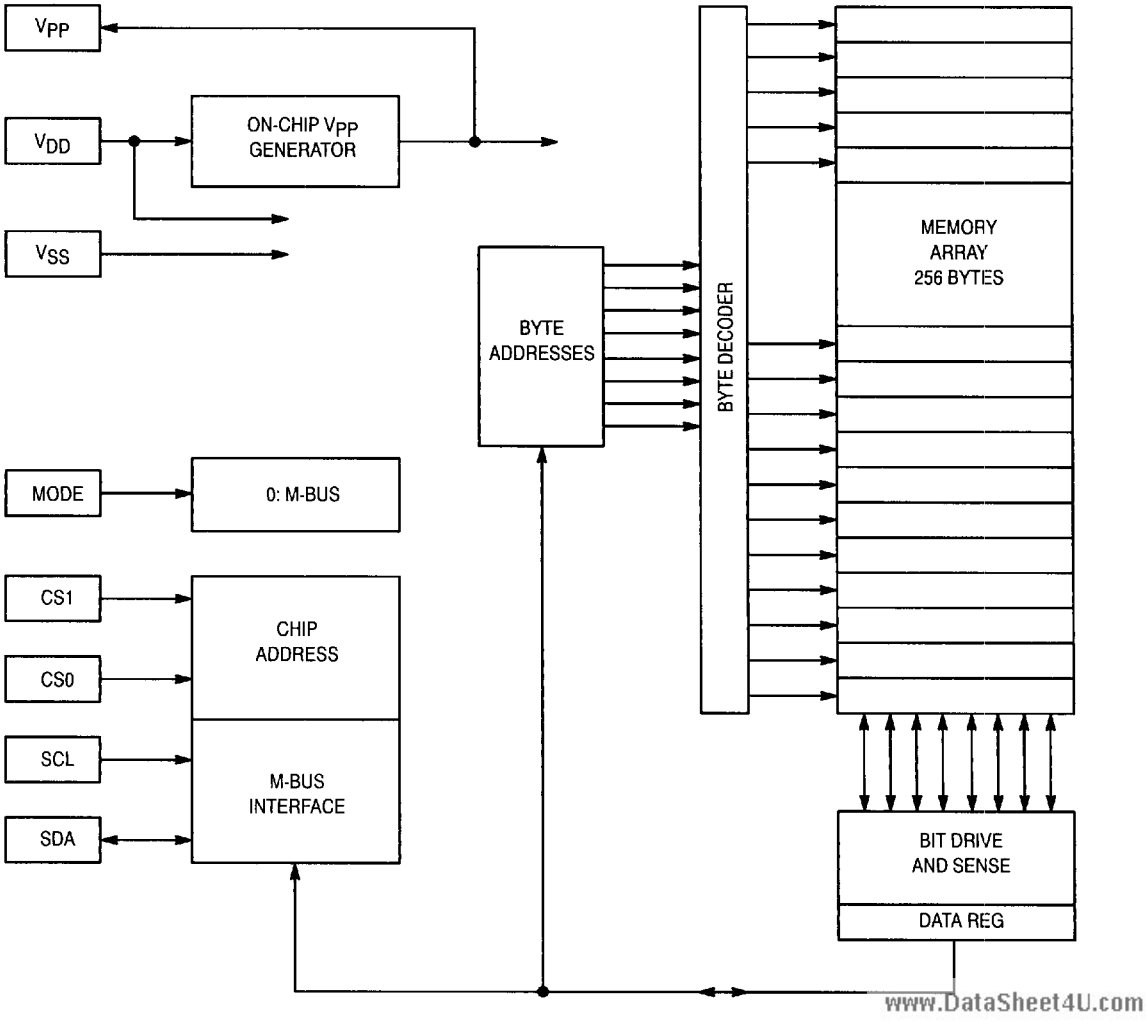
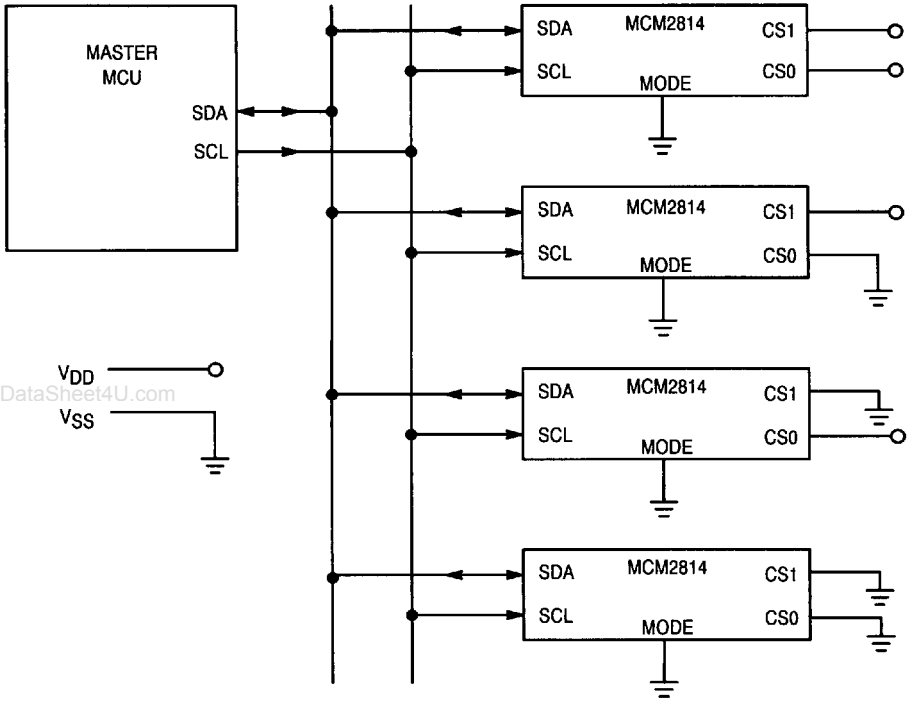


Figure 3. M-Bus Block Diagram

3.3 CHIP SELECTION

The two chip select bits transmitted in the chip address must match the status of CS1 and CS0 inputs.



PIN STATUS			CHIP ADDRESS
MODE	CS1	CS0	TRANSMITTED
0	1	1	1010 X11
0	1	0	1010 X10
0	0	1	1010 X01
0	0	0	1010 X00

Figure 4. M-Bus Chip Selection

3.4 PROTOCOL

At the protocol level, the transmission of data is defined in the form of sequences of Start (STA), Stop (STO) conditions, and bytes followed by acknowledge bits.

3.4.1 Standby State

When no serial transmission and no programming are made, the circuit is in standby. A STOP condition following a read sequence or a write byte address sequence (without data write), will put the circuit in standby. A new START condition will wake up the device, to get the chip address. If the chip address is not valid, the device will return to standby.

The power consumption is minimum in standby.

3.4.2 Write Sequence

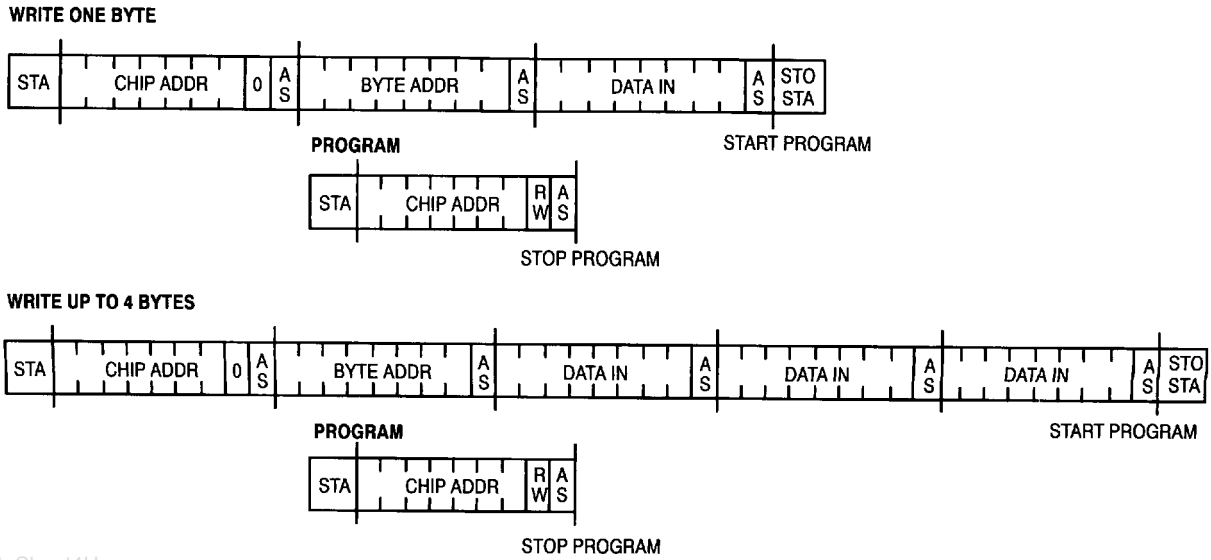
The serial write to the memory includes a serial transmission of the byte address and the data to be written. When this is completed by a stop or a new start condition, the programming sequence is initiated.

Programming is under control of the master. It is initiated by the write sequence just described, and stopped by any new valid selection of the chip. Therefore, the t_{PROG} time is defined as the time between these two operations, and is defined by the master.

Bad chip addresses or chip addresses for other chips on the same bus do not suspend the programming.

The on-chip V_{PP} generator is automatically turned on or off when needed. If an external V_{PP} is applied, the programming voltage is only allowed into the array during the above defined t_{PROG} time.

It is possible to program simultaneously up to 4 bytes, provided the 6 most significant bits of their addresses are identical. The byte address is incremented after each new data byte shifted in.



STA: Start Condition
STO: Stop Condition
R/W Bit: 1 = Read/0 = Write
INC: Increment Byte Address
AS: Slave Acknowledge (2814)
AM: Master Acknowledge

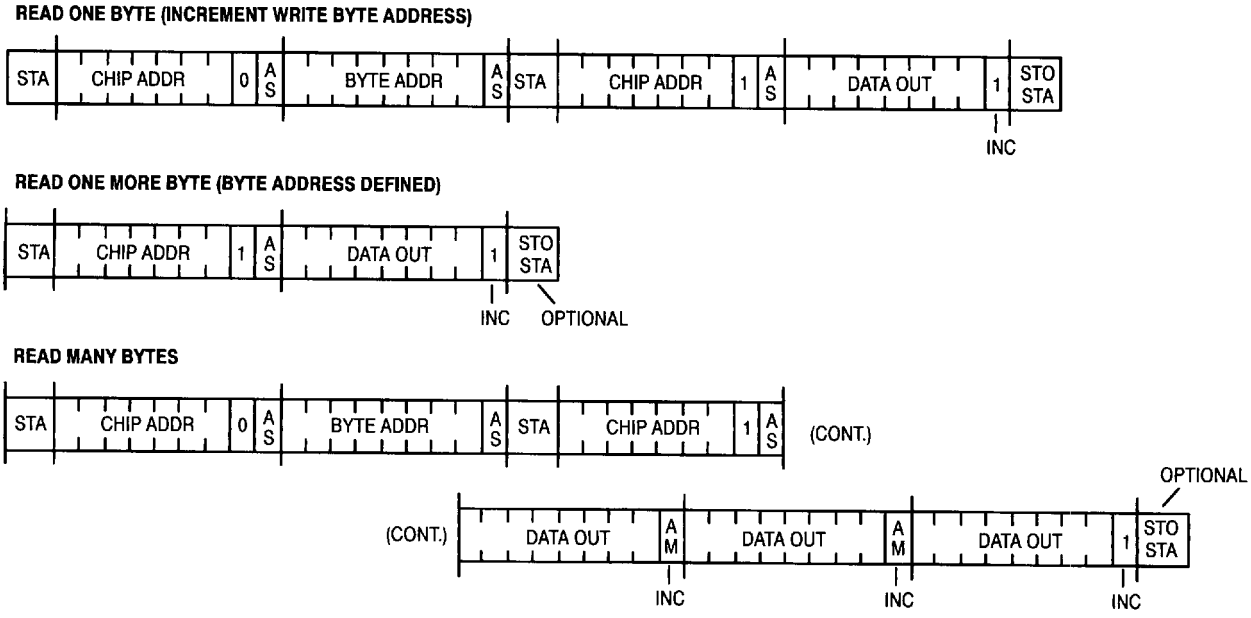
Figure 5. M-Bus Write Protocol

3.4.3 Read Sequence

Reading data from the memory is made in two steps. First the byte address must be loaded in the byte address register. Then data can be read out of the memory. The first step is only required to define the byte address. If this address was predefined from a previous read, this step can be skipped.

The byte address is automatically incremented after each data byte transmitted.

This is also valid after the last byte of a transmission. Therefore, the next read sequence without any byte address specified will transmit data of the next byte. A read sequence will transmit data bytes of successive addresses until the absence of the acknowledge bit from the master. In this case, the SDA output driver will switch off and the circuit will go to standby.



STA: Start Condition
STO: Stop Condition
R/W Bit: 1 = Read/0 = Write
INC: Increment Byte Address
AS: Slave Acknowledge (2814)
AM: Master Acknowledge

Figure 6. M-Bus Read Protocol

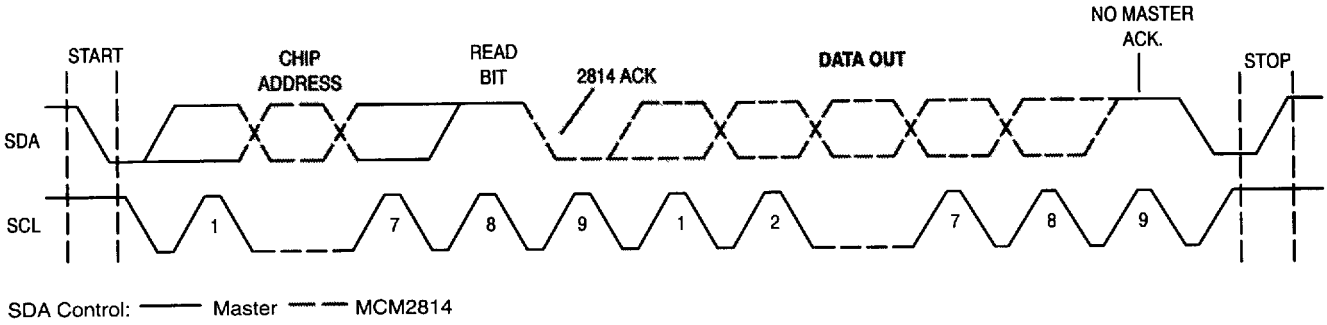


Figure 7. M-Bus Read Detail

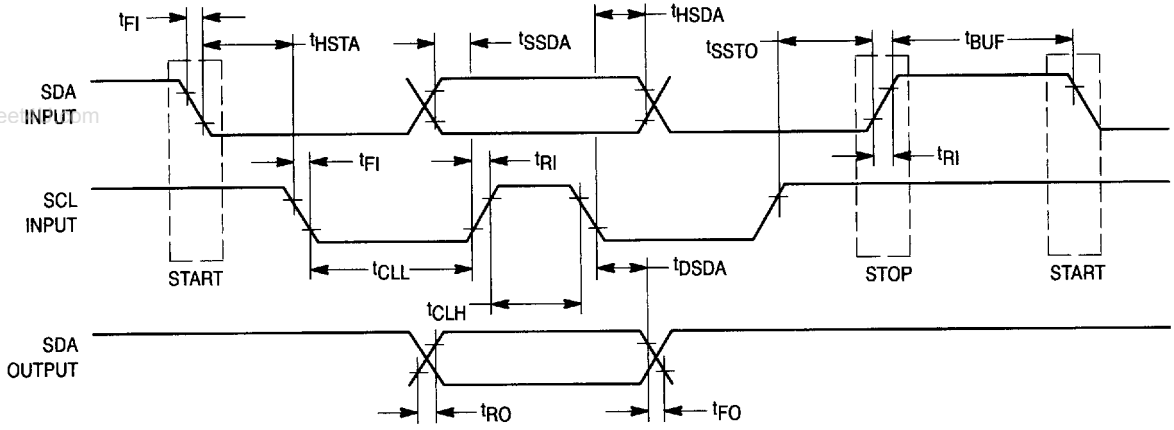


Figure 8. M-Bus Timings

3.4.4 Signal Levels

Electrical and switching characteristics are described in Section 5.

During a trasmission, SDA line transitions must occur when SCL is low. A negative transition of SDA with SCL high is recognized as a START condition, the positive transition as a STOP condition.

The acknowledge bit is provided by the device receiving data. Therefore, during this time the data transmitter must leave the SDA line at high impedance.

As this memory has an open drain SDA output, an external pull-up resistor to V_{DD} should be included on SDA line.

4. SPI OPERATING MODE

The serial transmission of this mode requires 4 wires to control the device operation. It features:

- Multiple chips on same 3 wire bus with separate chip select lines
- SPISS chip selection
- SPICK clock line, input only
- SPISI line used as input only
- SPISO line used as output only
- No acknowledge bit
- Programming under control of the master via serial op-codes
- Programming time under external control
- Write inhibit after reset
- Write enable/disable via serial opcodes
- Byte address output for transparency

This SPI mode can be used with the SPI of Motorola Microprocessor MC6805S2/S3, MC6805K2/L3/L8, MC68HC05C4, and MC68HC11.

4.1 SPI SERIAL INTERFACE

The serial interface via pins SPICL, SPISI, and SPISO is compatible with the SPI standard when the MODE pin is high.

4.2 LEXICON

This lexicon will describe some terms used in this serial interface description.

MASTER: The device that generates the serial clock on SPICK is designated as master. This memory can never function as a master.

SLAVE: This memory always operates as a slave as the SPICK pin is always an input.

TRANSMITTER/RECEIVER: This device has separate pins for data transmission (SPISO) and reception (SPISI). Simultaneous data input and output can therefore occur when the chip is selected with SPISS and is clocked (SPICK).

MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin SPISS is low. When the chip is not selected, no data will be input from pin SPISI, and output pin SPISO is high impedance.

4.3 SERIAL OP-CODE

The first byte transmitted after the chip is selected with SPISS going low, contains the opcode that defines the operation to be performed.

Table 2. SPI Opcodes

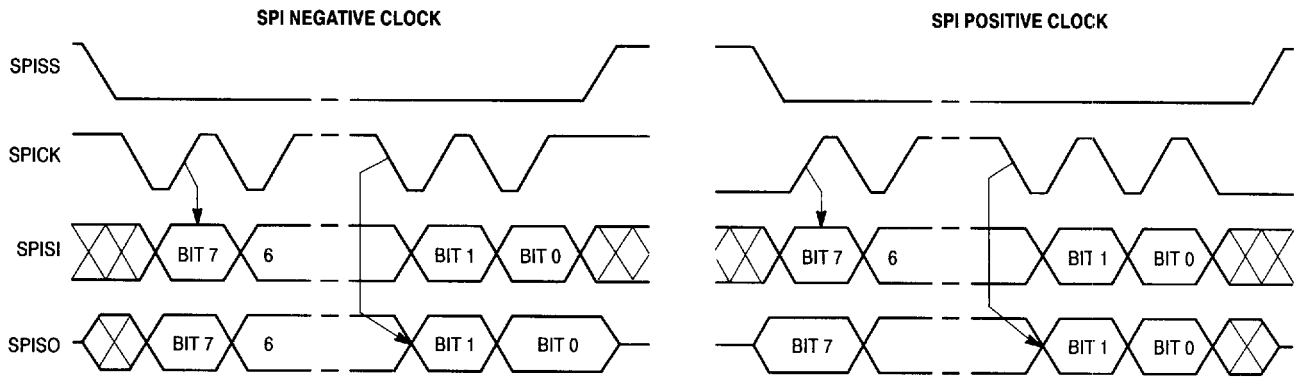
Data Transmitted		Operation
1010	0111	Read byte address followed by data
1010	0110	Program enable, V_{PP} generator ON.
1010	0100	Program disable, V_{PP} generator OFF.
1010	0010	Write (Program) data.

All other codes are invalid. After an invalid code is received, no data is shifted in the MCM2814 and the SPISO data output is high impedance until a new SPISS falling edge re-initializes the serial communication.

4.4 PROTOCOL

The MCM2814 SPI interface accepts both a negative or positive clock.

The SPI protocol for this device defines the bytes transmitted on the SPISI and SPISO data lines for proper chip operation.



Positive Clock Edge: Shift IN
Negative Clock Edge: Data OUT

Figure 9. SPI Clock Phase and Polarity

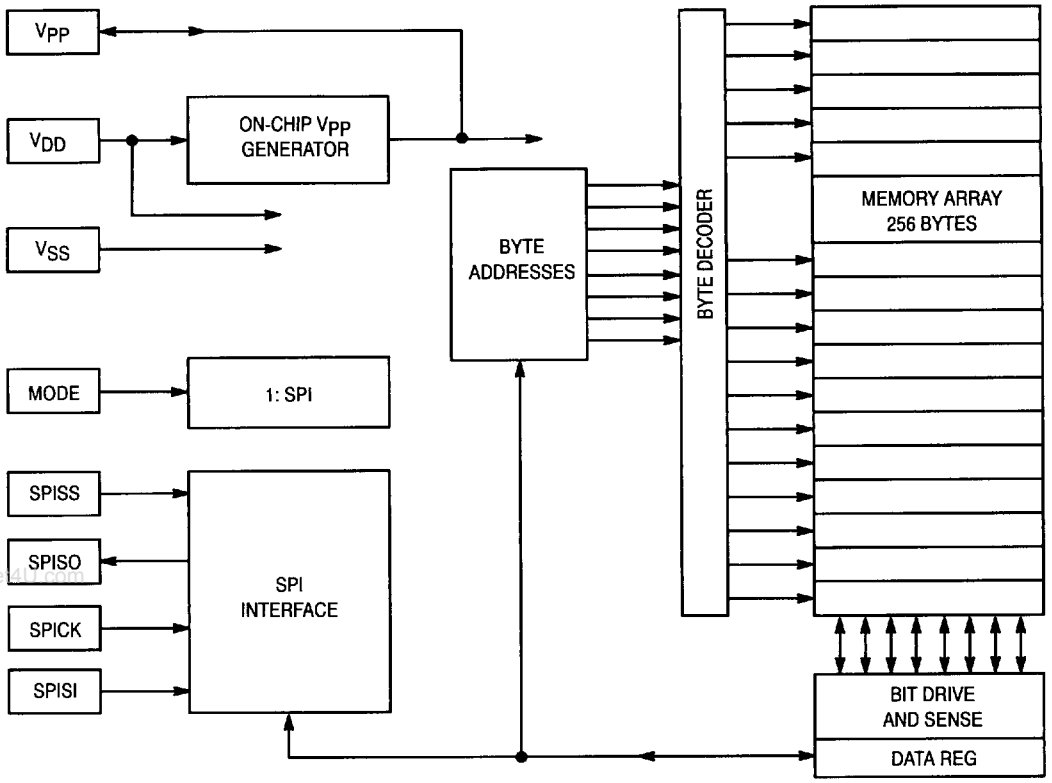


Figure 10. SPI Block Diagram

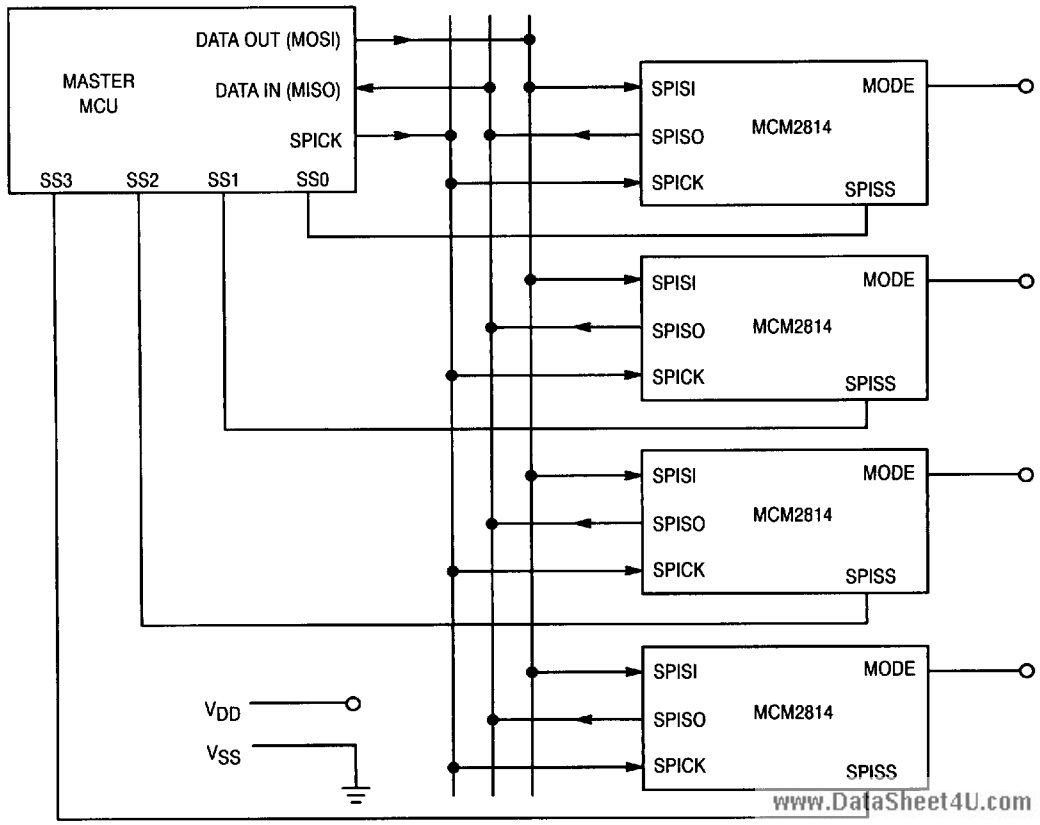


Figure 11. SPI Chip Selection

4.5 STANDBY STATE

The circuit is in standby when no serial transmission takes place, when no write is waiting for the V_{PP} enable command and when the V_{PP} generator is off.

When SPISS is high, standby state will follow:

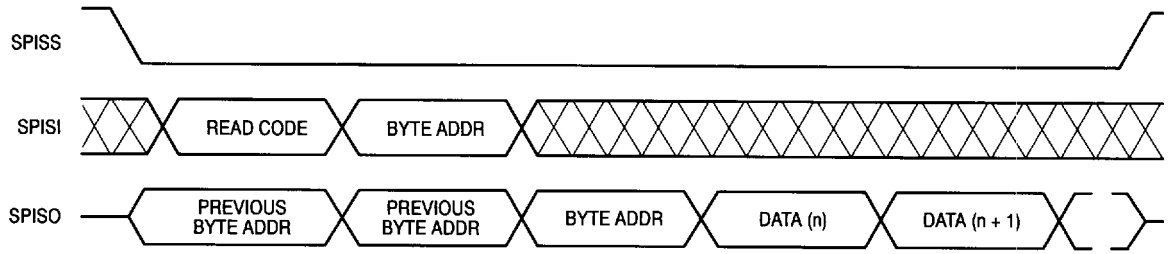
- A power up reset
- A V_{PP} disable command
- A Read, providing no V_{PP} enable command has been issued previously

The power consumption is minimum in standby.

4.6 READ SEQUENCE

Reading the memory via the serial SPI link requires the following sequence. The SPISS line is pulled low to select the device. The read opcode is transmitted on the the SPISI line followed by the byte address. When this is done, data on the SPISI line has no more influence on the memory. At the beginning of an SPI transaction, the SPISO buffer is turned on and will shift out the current byte address. This can be used for a relative addressing of the byte address. The new byte address is then transmitted followed by corresponding data. If just one byte is read, SPISS can be pulled back to the high level. It is possible to continue the read sequence, as the byte address is automatically incremented. The byte address is shifted out only once, in the beginning of a transmission.

READ ONE OR MORE BYTES



INVALID OPCODES

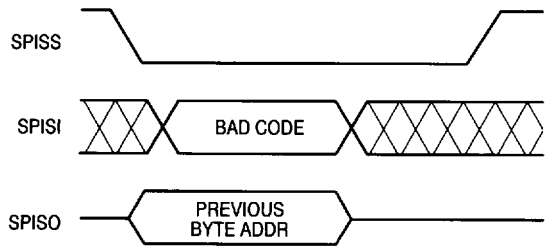


Figure 12. SPI Read

4.7 PROGRAM SEQUENCE

To program a byte, two separate conditions must be simultaneously present. The program must be enabled via the VPP enable command, and a serial write must be done. The VPP enable will also turn on the on-chip VPP generator. At this time, the chip is obviously not in standby, even if SPISS is high. The program disable command will stop the on-chip VPP supply and protect the EEPROM data against unwanted modifications. An external VPP supply will also be internally enabled or disabled by this mechanism.

A write serial sequence includes an SPISS high to low transition, followed by the write code on the SPISI line. The byte address followed by the corresponding data to be written are then shifted through the SPISI pin. At the beginning of an SPI transaction, the SPISO buffer is turned on and will shift out the current byte address. This can be used for a relative addressing of the byte to be programmed. The new byte address is also echoed for possible checking by the master. If VPP is enabled, the programming will start after the SPISS line goes back to a high level. It is also possible to issue the VPP enable command after the write sequence.

If the VPP enable command is issued after the serial write, no read or invalid code should be transmitted in between, as this would clear the programming latch containing the data to be programmed.

The programming is suspended when a new chip selection with SPISS low occurs. It is then possible to send a new write command to program new data. A VPP enable or a read command will stop the programming.

It is possible to program simultaneously up to 4 bytes, provided the 6 most significant bits of their addresses are identical. The byte address is incremented after each new data byte shifted in.

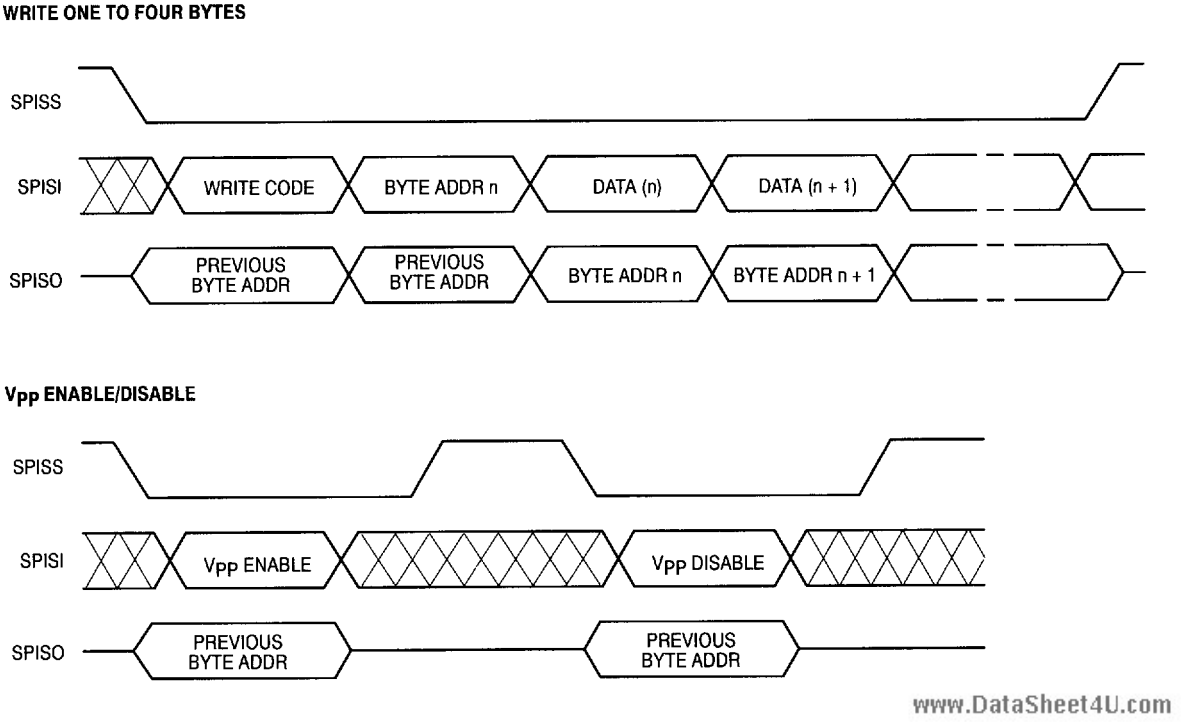


Figure 13. SPI Program

4.8 SIGNAL LEVELS

Electrical and switching characteristics are described in Section 5.

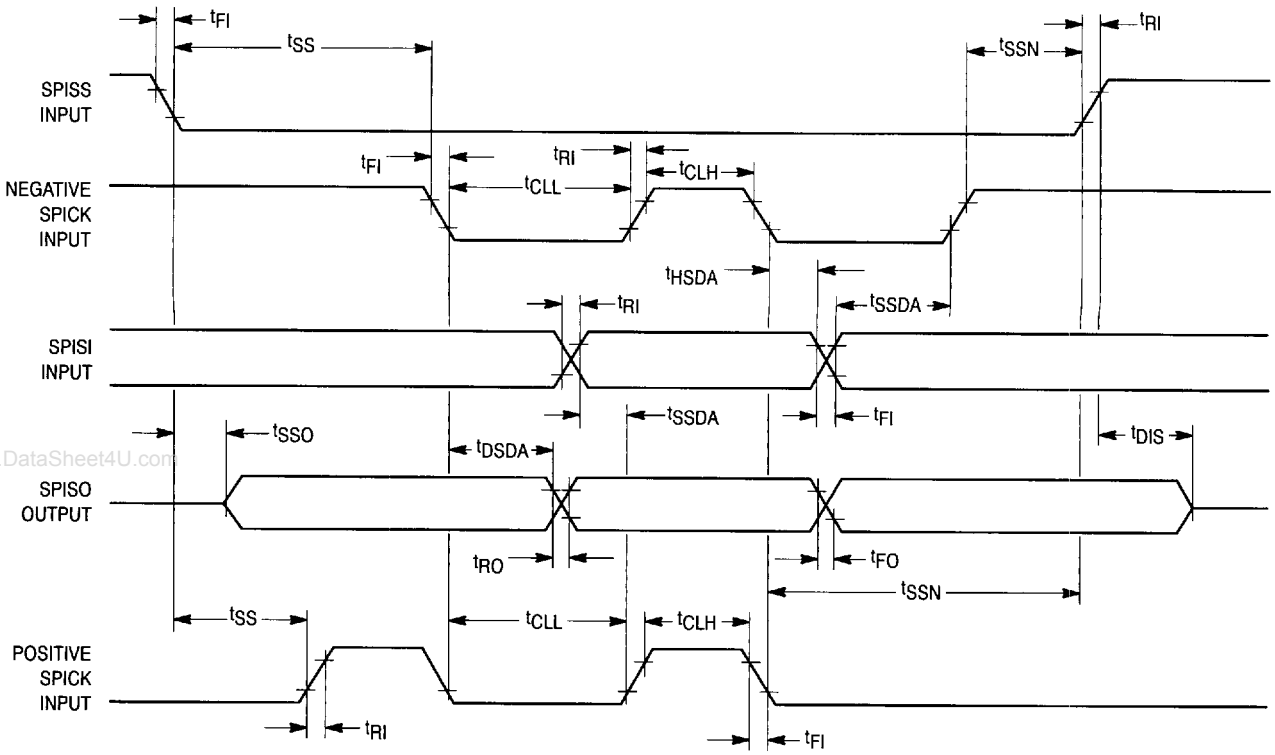


Figure 14. SPI Timing

5. CHARACTERISTICS

5.1 MAXIMUM RATINGS (V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	– 0.3 to + 7.0	V
Input Voltage Pins 1, 3, 5, 6	V_{in}	– 0.3 to + 7.0	V
Input Voltage Pin 2	V_{in}	– 0.3 to V_{DD} + 0.3	V
Current on any Input	I_{in}	0.1	mA
Sink Current SDA	I_{SDAL}	10	mA
Sink Current SPISO	I_{SOL}	10	mA
Source Current SPISO	I_{SOH}	10	mA
Operating Temperature	T_A	0 to 70*	°C
Storage Temperature	T_S	– 55 to 125**	°C
Junction Temperature	T_j	150**	°C
Thermal Resistance	Th_{ja}	200	°C/W

*Specification over the temperature range, – 40 to + 125°C to be determined.

** In particular, continuous high temperature application may cause leakage of store charge in EEPROM, resulting in data loss.

NOTE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum operating conditions for extended periods may affect reliability.

5.2 ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage STANDBY	V_{DDS}	—	—	6.0	V
Supply Current STANDBY*	I_{DDS}	—	0.5	1.0	µA
Supply Voltage READ	V_{DDR}	3.0	—	6.0	V
Supply Current READ*	I_{DDR}	—	0.3	1.5	mA
Supply Voltage PROG	V_{DDP}	3.0**	—	6.0	V
Supply Current PROG*	I_{DDP}	—	0.5	3.0	mA

*Inputs at V_{SS} or V_{DD}.
**3 V device only. Standard is 4.5 V.

5.3 ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
SCL, SDA, SPISS, SPISI Inputs	Input Low Voltage	V_{IL}	– 0.3	—	0.3 x V_{DD}	V
	Input High Voltage	V_{IH}	0.7 x V_{DD}	—	V_{DD} + 0.3	V
	Input Leakage	I_{in}	—	—	± 10	µA
SDA/SPISO Pull Down Outputs	Output Low I_{OL} < 10 µA	V_{OL}	—	—	0.1	V
	Output High Leakage	I_{OH}	—	—	± 10	µA
	Output Low I_{OL} = 3 mA, V_{DD} = 5 V	V_{OL}	—	—	0.4	V
	Output Low I_{OL} = 1 mA, V_{DD} = 3 V	V_{OL}	—	—	0.4	V
SPISO Pull Up Output	Output High I_{OH} = 1.6 mA, V_{DD} = 5 V	V_{OH}	V_{DD} – 0.8	—	—	V
	Output High I_{OH} = 0.4 mA, V_{DD} = 3 V		V_{DD} – 0.3	—	—	
MODE, CS1, CS0 Inputs	Input Low Voltage	V_{IL}	– 0.3	—	0.3 x V_{DD}	V
	Input High Voltage	V_{IH}	0.7 x V_{DD}	—	V_{DD} + 0.3	V
	Input Leakage	I_{in}	—	—	± 10	µA
Input Capacitance		C_{in}	—	10	—	pF

5.4 SWITCHING PARAMETERS

5.4.1 General Characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Programming Time	1 Byte	t_{PROG}	10	—	—	ms
	4 Bytes		20	—	—	
Write/Erase	0 to 70°C	$cy_{W/E}$	—	—	10,000	cycles
	Ambient Temperature		—	100,000	—	

5.4.2 Serial Bus Input

Characteristic		Symbol	Min	Typ	Max	Unit
SDA/SPISI, SCL/SPICK, SPISS Inputs	Clock Frequency	F_{SCL}	0.0	—	125	kHz
	Clock High Time	t_{CLH}	4.0	—	—	µs
	Clock Low Time	t_{CLL}	4.0	—	—	µs
	Stop to Start Delay	t_{BUF}	4.0	—	—	µs
	Start Hold Time	t_{HSTA}	4.0	—	—	µs
	Data Hold Time	t_{HSDA}	0.0	—	—	µs
	Data Set-Up Time	t_{SSDA}	250	—	—	ns
	Input Rise Time	t_{RI}	—	—	1.0	µs
	Input Fall Time	t_{FI}	—	—	300	ns
	Stop Set-Up Time	t_{SSTO}	4.0	—	—	µs
	SPISS Lead Time	t_{SS}	4.0	—	—	µs
	SPISS Lag Time	t_{SSN}	4.0	—	—	µs

NOTE: All values refer to V_{IH} and V_{IL} levels.

5.4.3 Serial Bus Output

Characteristic	Symbol	Min	Typ	Max	Unit
SDA/SPISO Outputs (V_{DD} = 5 V ± 10%, T_A = 0 to 70°C, C_L = 200 pF)					
Data Delay	t_{DSDA}	—	1.5	3.5	µs
Rise Time SDA	t_{RO}	—	—	*	ns
Rise Time SPISO	t_{RO}	—	—	100	ns
Fall Time	t_{FO}	—	—	100	ns
SPI Select Time	t_{SSO}	—	—	1.2	µs
Disable Time	t_{DIS}	—	1.5	3.5	µs
SDA/SPISO Outputs (V_{DD} = 3.3 V ± 10%, T_A = 0 to 70°C, C_L = 200 pF)					
Data Delay	t_{DSDA}	—	2.0	3.5	µs
Rise Time SDA	t_{RO}	—	—	*	ns
Rise Time SPISO	t_{RO}	—	—	200	ns
Fall Time	t_{FO}	—	—	200	ns
SPI Select Time	t_{SSO}	—	—	1.5	µs
Disable Time	t_{DIS}	—	2.0	3.5	µs

NOTE: All values refer to V_{IH} and V_{IL} levels.
*Depends on external pull-up resistor value where $t_{RI} = C_{bus}/R_{pull\text{-}up}$.

ORDERING INFORMATION
(Order by Full Part Number)

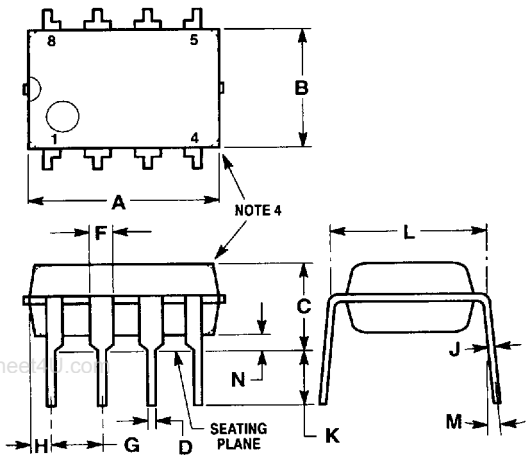
MCM 2814 X X

- MCM — Motorola Memory Prefix
- 2814 — Part Number
- X — Package (BP = 300 mil DIP, G = 150 mil SOG)
- X — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM2814BP
MCM2814G
MCM2814GR2

PACKAGE DIMENSIONS

BP SUFFIX
PLASTIC PACKAGE
CASE 626-04



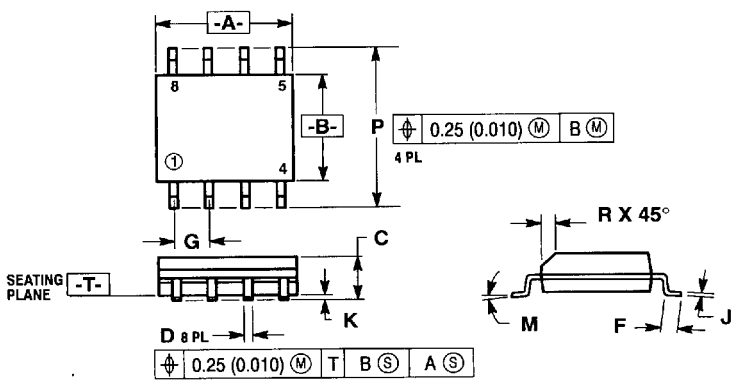
NOTES:
1. LEAD POSITIONAL TOLERANCE

⌖	ϕ 0.13 (0.005) Ⓜ	T	A Ⓜ	B Ⓜ

2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS)
4. DIMENSIONS A AND B ARE DATUMS
5. DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9 40	10 16	0 370	0 400
B	6 10	6 60	0 240	0.260
C	3 94	4 45	0 155	0.175
D	0.38	0 51	0.015	0 020
F	1.02	1.52	0 040	0 060
G	2 54 BSC		0.100 BSC	
H	0 76	1 27	0 030	0 050
J	0 20	0 30	0 008	0 012
K	2 92	3 43	0 115	0 135
L	7 62 BSC		0 300 BSC	
M	—	10°	—	10°
N	0 51	0 76	0 020	0 030

G SUFFIX
PLASTIC PACKAGE
CASE 751-03



NOTES
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE
2. DIMENSIONING AND TOLERANCING PER ANSI Y14 5M, 1982
3. CONTROLLING DIM MILLIMETER
4. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION
5. MAXIMUM MOLD PROTRUSION 0 15 (0 006) PER SIDE
6. 751-01 AND -02 OBSOLETE, NEW STANDARD 751 03

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4 80	5 00	0.189	0 196
B	3 80	4 00	0 150	0 157
C	1 35	1.75	0 054	0 068
D	0 35	0 49	0 014	0 019
F	0 40	1 25	0 016	0 049
G	1 27 BSC		0 050 BSC	
J	0 18	0 25	0 007	0 009
K	0 10	0 25	0 004	0 009
M	0°	7°	0°	7°
P	5 80	6 20	0 229	0 244
R	0 25	0 50	0 010	0 019

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