# FSW25N50A

N-Channel MOSFET

Lead Free Package and Finish

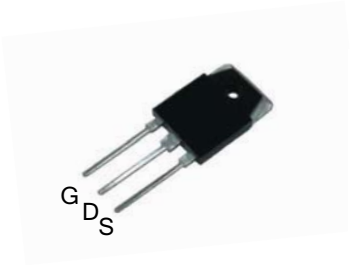
## Applications:

- Uninterruptible Power Supply(UPS)
- LCD Panel Power
- SMPS Power
- DC-AC Inverter

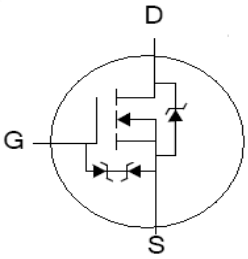
| $V_{DSS}$ | $R_{DS(ON)}$ (Typ.) | $I_D$ |
|---|---|---|
| 500V | 0.18 Ω | 25A |

## FSW25N50

- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- ESD Capability Improved




TO-3PN
Not to Scale




### Ordering Information

| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| FSW25N50A | TO-3PN | FSW25N50A |

### Absolute Maximum Ratings $T_C$=25 °C unless otherwise specified

| Symbol | Parameter | FSW25N50A | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-to-Source Voltage (NOTE *1) | 500 | V |
| $I_D$ | Continuous Drain Current | 25 | A |
| $I_D$@ 100 °C | Continuous Drain Current | Figure 3 | |
| $I_{DM}$ | Pulsed Drain Current, $V_{GS}$@ 10V (NOTE *2) | Figure 6 | |
| $P_D$ | Power Dissipation | 230 | W |
| | Derating Factor above 25 °C | 1.84 | W/ °C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 30 | V |
| $E_{AS}$ | Single Pulse Avalanche Engergy L=10mH | 2500 | mJ |
| $I_{AS}$ | Pulsed Avalanche Rating | Figure 8 | |
| dv/dt | Peak Diode Recovery dv/dt (NOTE *3) | 5.0 | V/ns |
| VESD(G-S) | Gate to Source ESD:HBM_C=100pF,R=1.5KΩ | 6000 | V |
| $T_L$<br>$T_{PKG}$ | Maximum Temperature for Soldering<br>Leads at 0.063in (1.6mm) from Case for 10 seconds<br>Package Body for 10 seconds | <br>300<br>260 | °C |
| $T_J$ and $T_{STG}$ | Operating Junction and Storage Temperature Range | -55 to 150 | |

**Drain Current limited by Maximum Junction Temperature.*
***Caution:** Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.*

### Thermal Resistance

| Symbol | Parameter | FSW25N50A | Units | Test Conditions |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | 0.54 | °C/W | Water cooled heatsink, $P_D$ adjusted for a peak junction temperature of +150 °C. |
| $R_{\theta JA}$ | Junction-to-Ambient | 62 | | 1 cubic foot chamber, free air. |

## OFF Characteristics $T_J$=25°C unless otherwise specified

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 500 | -- | -- | V | $V_{GS}$=0V, $I_D$=250μA |
| $\Delta BV_{DSS}/\Delta T_J$ | BreakdownVoltage Temperature Coefficient, Figure 11. | -- | 0.60 | -- | V/°C | Reference to 25°C, $I_D$=250μA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | -- | -- | 10 | μA | $V_{DS}$=500V, $V_{GS}$=0V |
| | | -- | -- | 250 | | $V_{DS}$=400V, $V_{GS}$=0V $T_J$=125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | -- | -- | +10 | uA | $V_{GS}$=+30V |
| | Gate-to-Source Reverse Leakage | -- | -- | -10 | | $V_{GS}$= -30V |

## ON Characteristics $T_J$=25°C unless otherwise specified

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $R_{DS(ON)}$ | Static Drain-to-Source On-Resistance Figure 9 and 10. | -- | 0.18 | 0.26 | Ω | $V_{GS}$=10V, $I_D$=10A (NOTE *4) |
| $V_{GS(TH)}$ | Gate Threshold Voltage, Figure 12. | 2.0 | -- | 4.0 | V | $V_{DS}$=$V_{GS}$, $I_D$=250μA |
| gfs | Forward Transconductance | -- | 24 | -- | S | $V_{DS}$=15V, $I_D$=10A (NOTE *4) |

## Dynamic Characteristics Essentially independent of operating temperature

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input Capacitance | -- | 4900 | -- | pF | $V_{GS}$=0V $V_{DS}$=25V f=1.0MHz Figure 14 |
| $C_{oss}$ | Output Capacitance | -- | 410 | -- | | |
| $C_{rss}$ | Reverse Transfer Capacitance | -- | 44 | -- | | |
| $Q_g$ | Total Gate Charge | -- | 96 | -- | nC | $V_{DD}$=250V $I_D$=20A $V_{GS}$=10V Figure 15 |
| $Q_{gs}$ | Gate-to-Source Charge | -- | 18 | -- | | |
| $Q_{gd}$ | Gate-to-Drain (“Miller”) Charge | -- | 41 | -- | | |

## Resistive Switching Characteristics Essentially independent of operating temperature

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $t_{d(ON)}$ | Turn-on Delay Time | -- | 53 | -- | ns | $V_{DD}$=250V $I_D$=20A $V_{GS}$=10V $R_G$=25Ω |
| $t_{rise}$ | Rise Time | -- | 117 | -- | | |
| $t_{d(OFF)}$ | Turn-Off Delay Time | -- | 307 | -- | | |
| $t_{fall}$ | Fall Time | -- | 138 | -- | | |

**Source-Drain Diode Characteristics** $T_C$=25°C unless otherwise specified

| Symbol | Parameter | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | -- | -- | 25 | A | Integral pn-diode in MOSFET |
| $I_{SM}$ | Maximum Pulsed Current (Body Diode) | -- | -- | 100 | A | |
| $V_{SD}$ | Diode Forward Voltage | -- | -- | 1.5 | V | $I_S$=20A, $V_{GS}$=0V |
| $t_{rr}$ | Reverse Recovery Time | -- | 558 | -- | ns | $V_{GS}$=0V |
| $Q_{rr}$ | Reverse Recovery Charge | -- | 6.1 | -- | μC | $I_F$=20A, di/dt=100 A/μs |

Notes:

*1. $T_J$ = +25°C to +150°C.

*2. Repetitive rating; pulse width limited by maximum junction temperature.

*3. $I_{SD}$= 20A di/dt ≤ 100 A/μs, $V_{DD}$ ≤ $BV_{DSS}$, $T_J$=+150°C.

*4. Pulse width ≤ 380μs; duty cycle ≤ 2%.

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

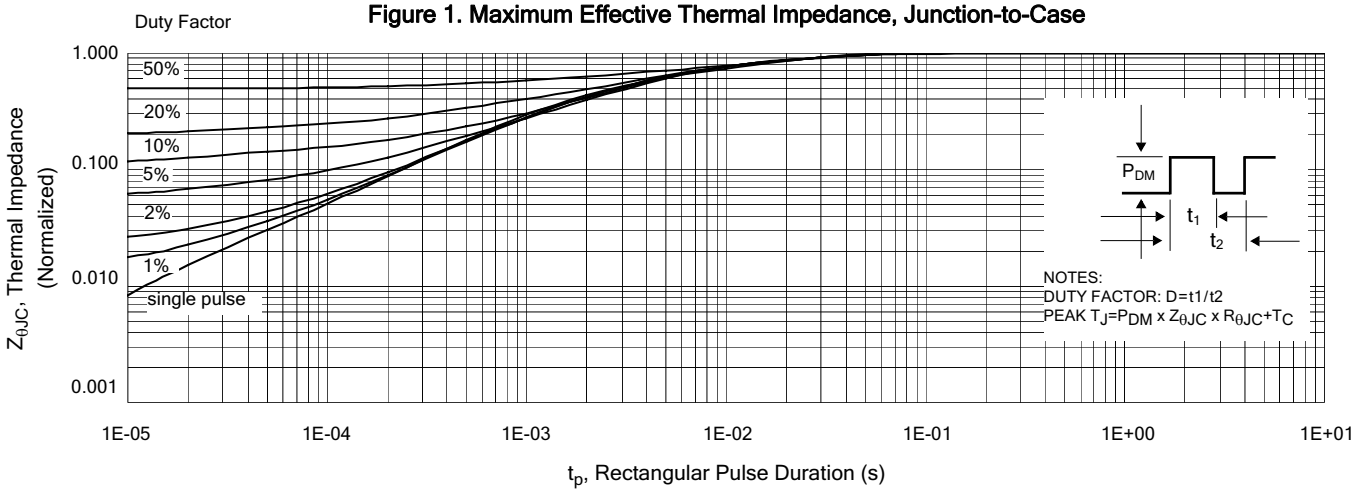



Figure 2. Maximum Power Dissipation vs Case Temperature

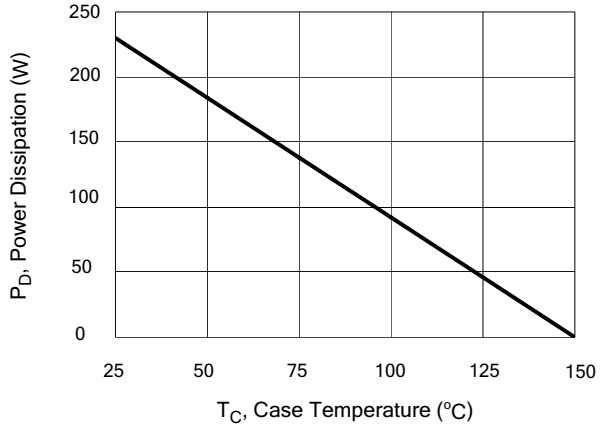



Figure3. Maximum Continuous Drain Current vs Case Temperature

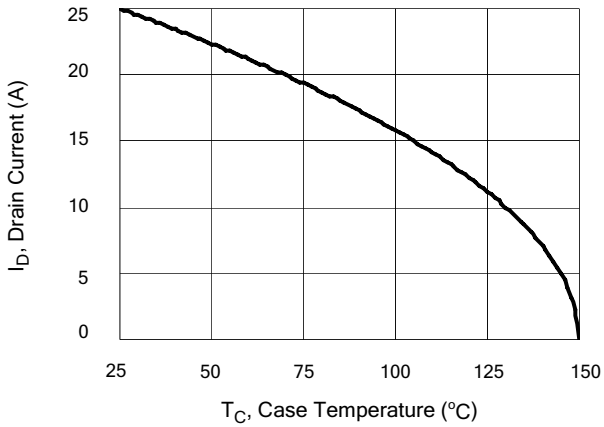



Figure 4. Typical Output Characteristics

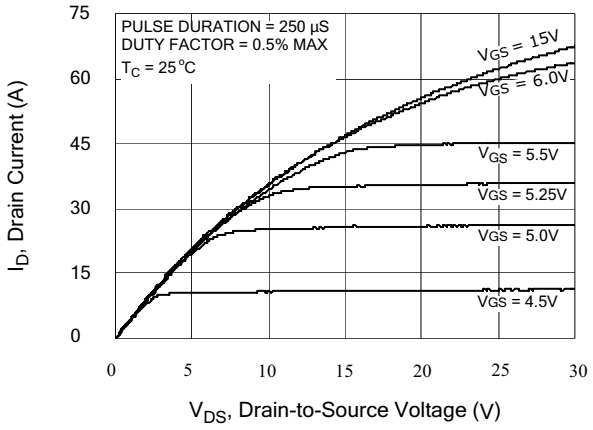



Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

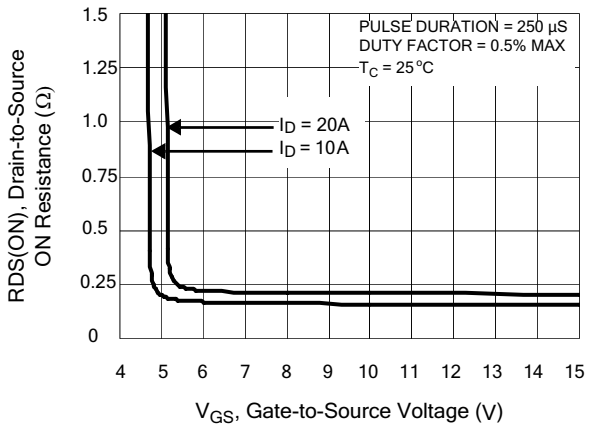


**Figure 6. Maximum Peak Current Capability**

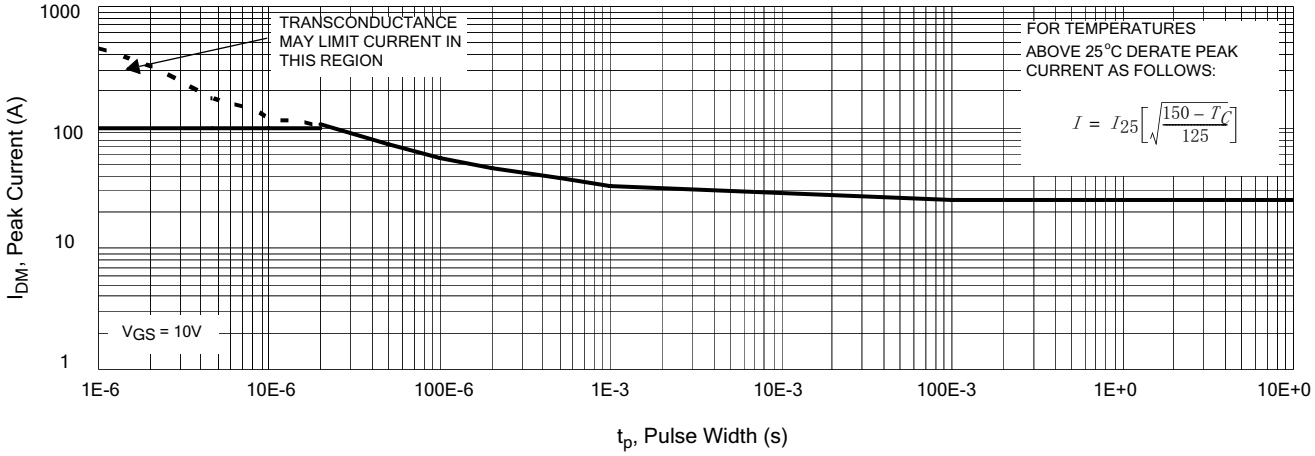



**Figure 7. Typical Transfer Characteristics**

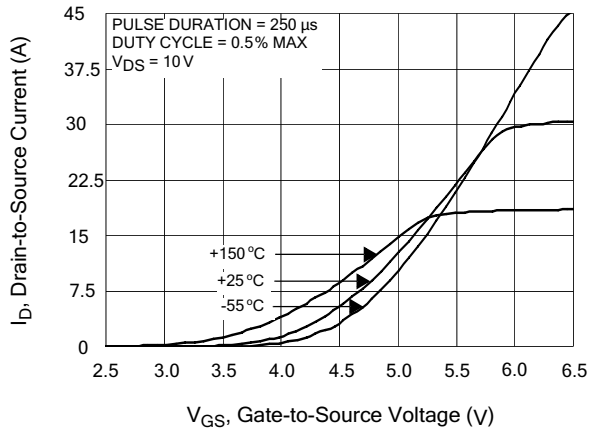



**Figure8. Unclamped Inductive Switching Capability**

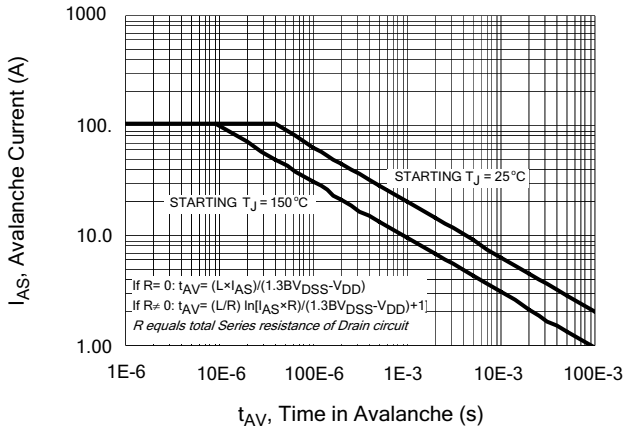



**Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current**

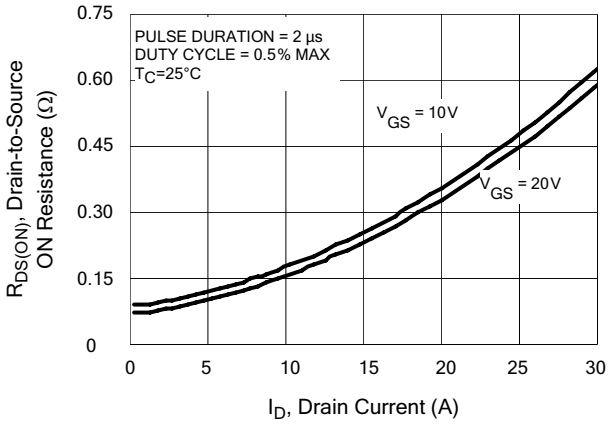



**Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature**

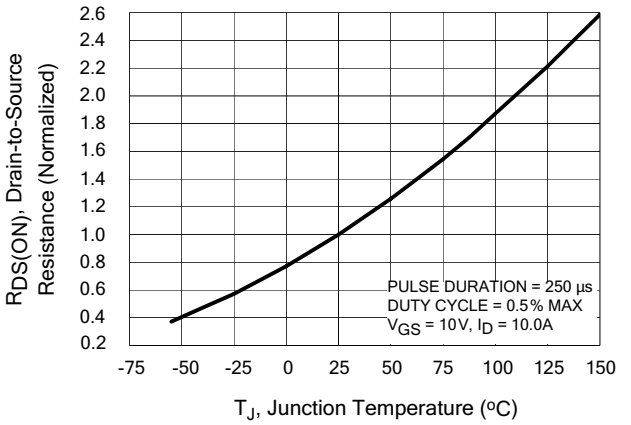


**Figure 11. Typical Breakdown Voltage vs Junction Temperature**

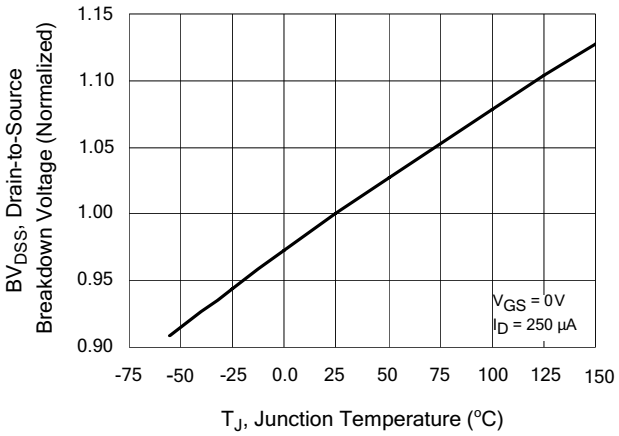



**Figure 12. Typical Threshold Voltage vs Junction Temperature**

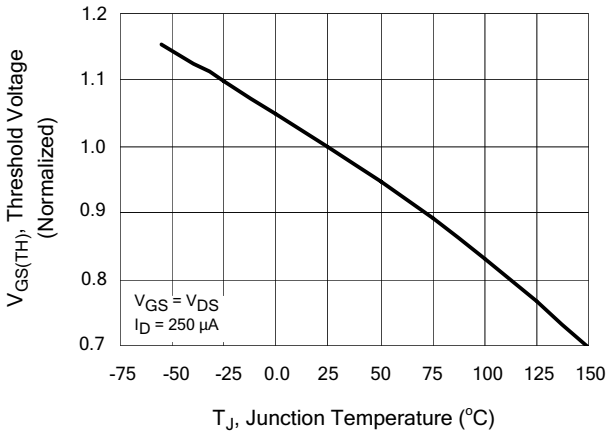



**Figure 13. Maximum Forward Bias Safe Operating Area**

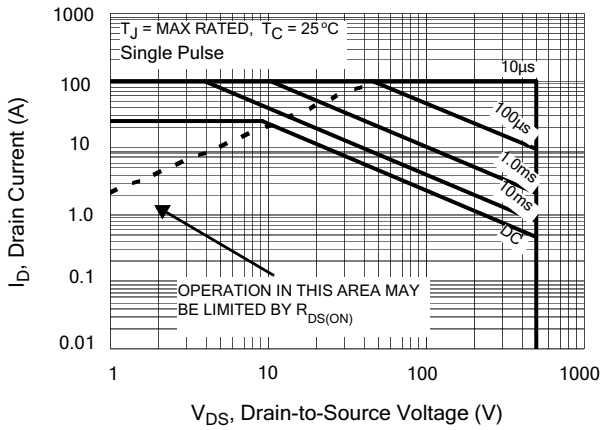



**Figure 14. Typical Capacitance vs**

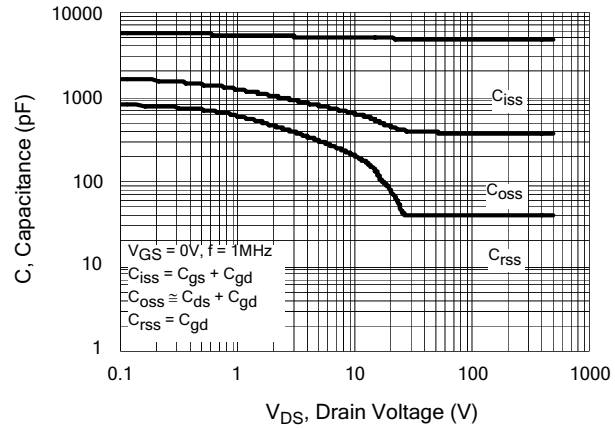



**Figure 15. Typical Gate Charge vs Gate-to-Source Voltage**

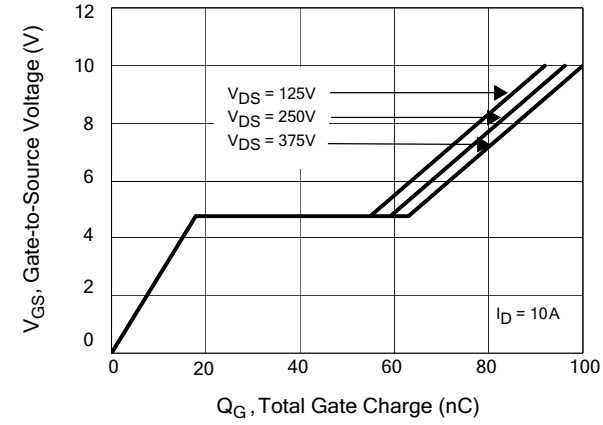
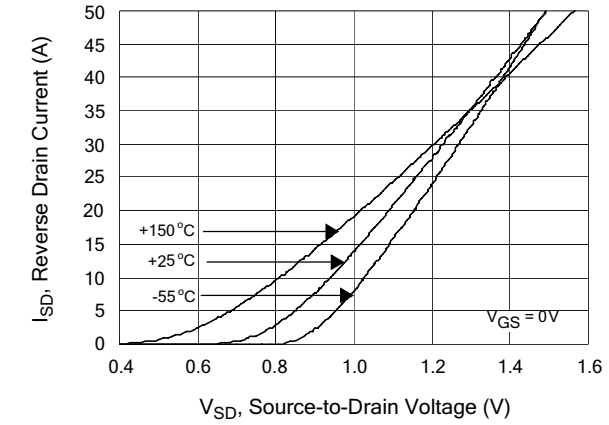



**Figure 16. Typical Body Diode Transfer Characteristics**



## Test Circuits and Waveforms

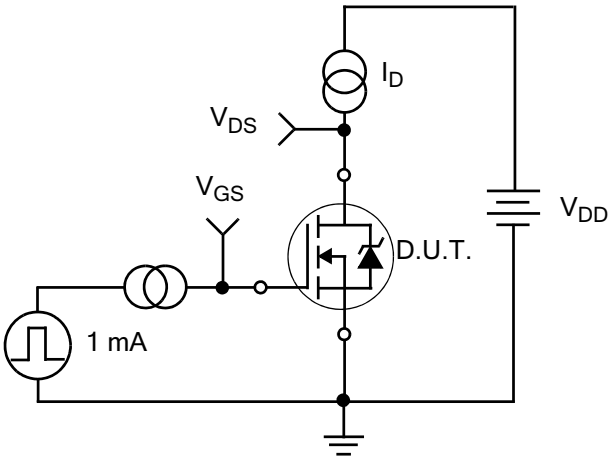



Figure 17. Gate Charge Test Circuit

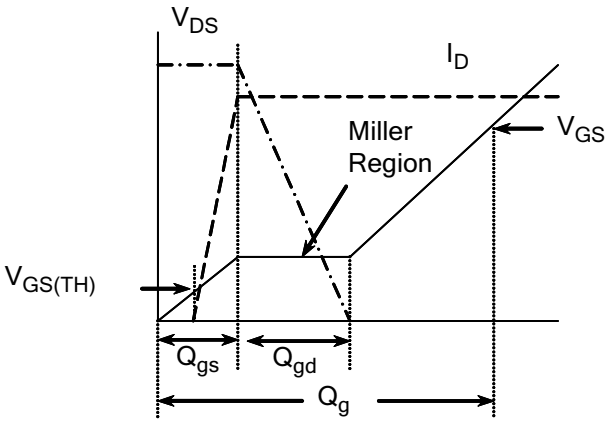



Figure 18. Gate Charge Waveform

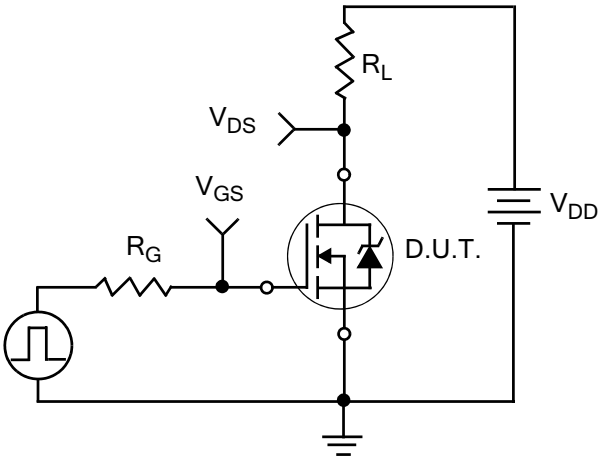



Figure 19. Resistive Switching Test Circuit

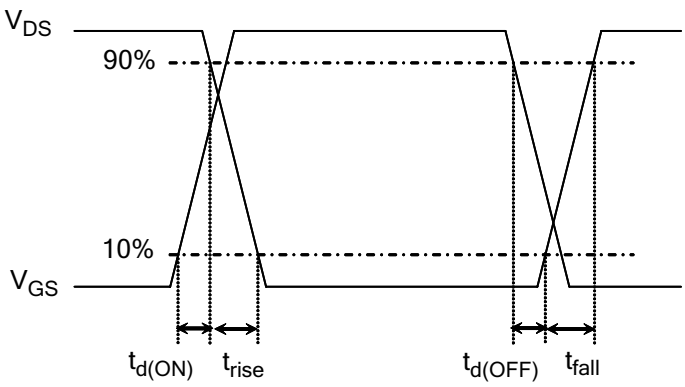



Figure 20. Resistive Switching Waveforms

## Test Circuits and Waveforms

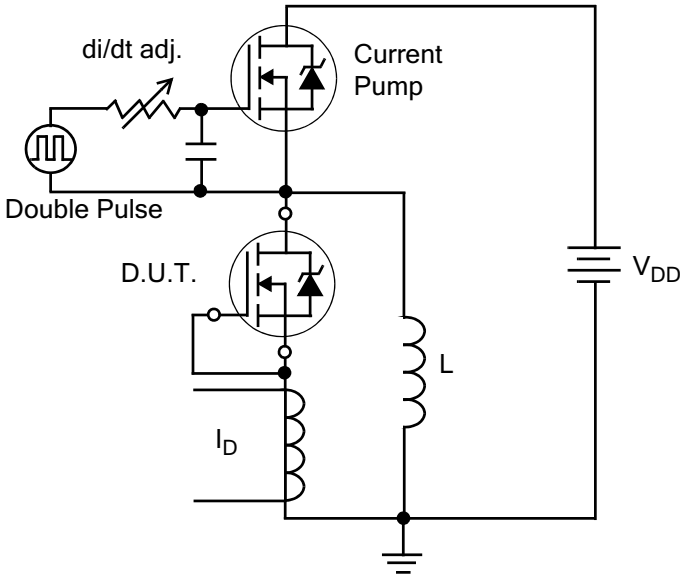



Figure 21. Diode Reverse Recovery Test Circuit

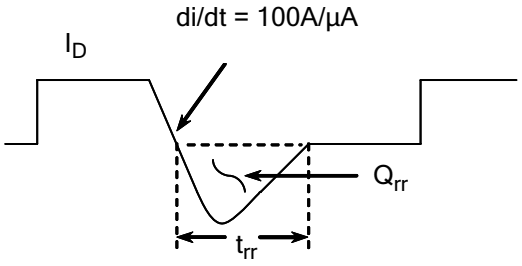



Figure 22. Diode Reverse Recovery Waveform

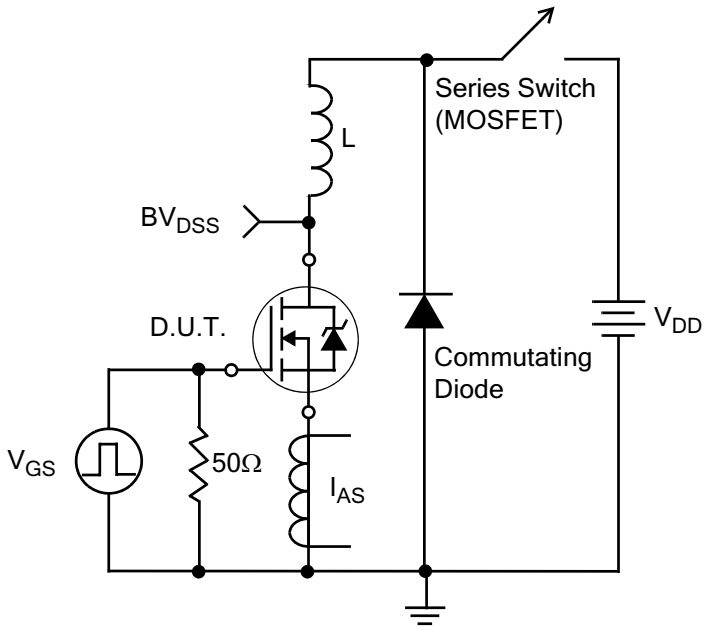
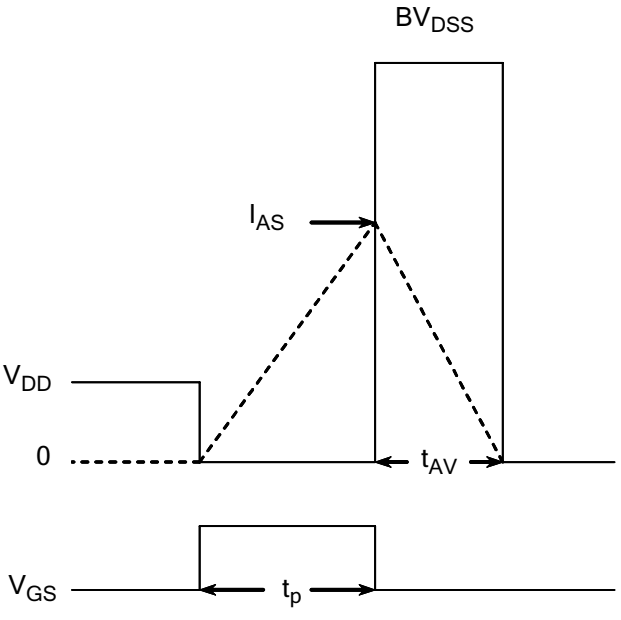



Figure 23. Unclamped Inductive Switching Test Circuit




$$E_{AS} = \frac{I_{AS}{}^2 L}{2}$$

Figure 24. Unclamped Inductive Switching Waveforms

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