



April 2016

FQD18N20V2

N-Channel QFET[®] MOSFET

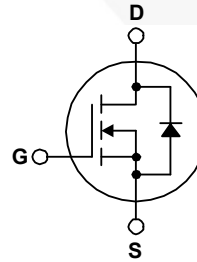
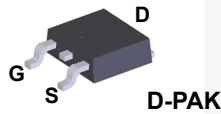
200 V, 15 A, 140 mΩ

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 15 A, 200 V, $R_{DS(on)} = 140 \text{ m}\Omega$ (Max.) @ $V_{GS} = 10 \text{ V}$, $I_D = 7.5 \text{ A}$
- Low Gate Charge (Typ. 20 nC)
- Low Crss (Typ. 25 pF)
- 100% Avalanche Tested



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQD18N20V2TM	Unit
V_{DSS}	Drain-Source Voltage	200	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	15	A
		9.75	A
I_{DM}	Drain Current - Pulsed (Note 1)	60	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	340	mJ
I_{AR}	Avalanche Current (Note 1)	15	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	8.3	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	83	W
	- Derate above 25°C	0.67	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FQD18N20V2TM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in ² Pad of 2-oz Copper), Max.	50	

FQD18N20V2 — N-Channel QFET[®] MOSFET

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD18N20V2TM	DV218N20	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	200	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.25	--	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 160\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 7.5\text{ A}$	--	0.12	0.14	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 7.5\text{ A}$	--	11	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	830	1080	pF
C_{oss}	Output Capacitance		--	200	260	pF
C_{riss}	Reverse Transfer Capacitance		--	25	33	pF
C_{oss}	Output Capacitance	$V_{DS} = 160\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	70	--	pF
$C_{oss\ eff.}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 160\text{ V}, V_{GS} = 0\text{ V}$	--	135	--	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 100\text{ V}, I_D = 18\text{ A},$ $R_G = 25\ \Omega$	--	16	40	ns	
t_r	Turn-On Rise Time		--	133	275	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	--	38	85	ns
t_f	Turn-Off Fall Time		(Note 4)	--	62	135	ns
Q_g	Total Gate Charge	$V_{DS} = 160\text{ V}, I_D = 18\text{ A},$ $V_{GS} = 10\text{ V}$	--	20	26	nC	
Q_{gs}	Gate-Source Charge		(Note 4)	--	5.6	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4)	--	10	--	nC
R_G	Gate Resistance	$f = 1\text{ MHz}$	0.5	--	2.5	Ω	

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	15	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	60	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 15\text{ A}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 18\text{ A},$ $dI_F / dt = 100\text{ A}/\mu\text{s}$	--	158	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.0	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. $L = 1.58\text{ mH}, I_{AS} = 18\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 18\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

Typical Characteristics

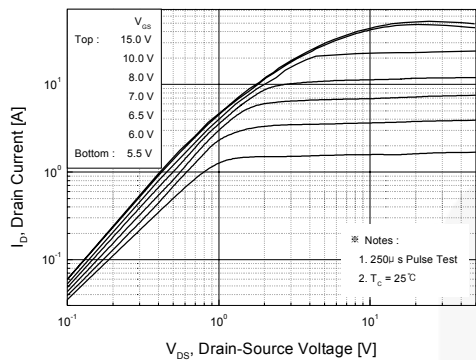


Figure 1. On-Region Characteristics

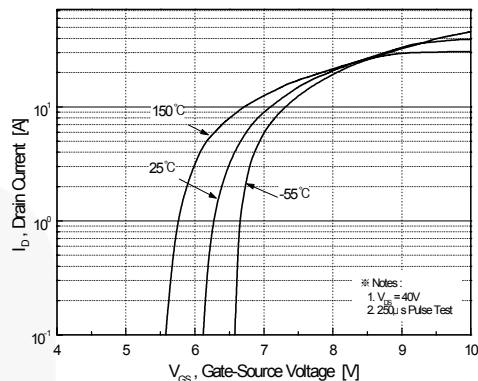


Figure 2. Transfer Characteristics

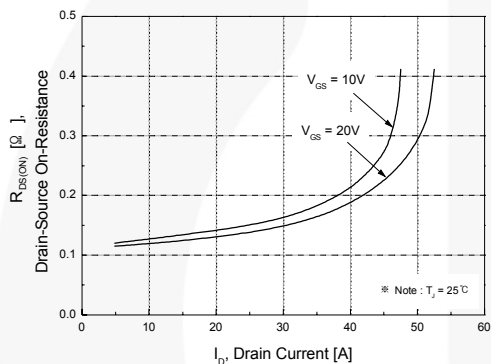


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

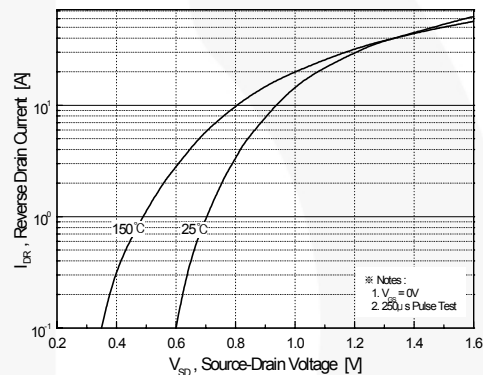


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

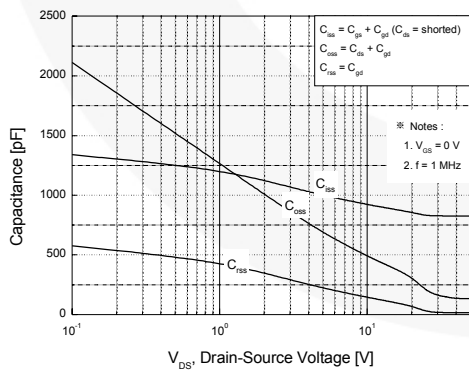


Figure 5. Capacitance Characteristics

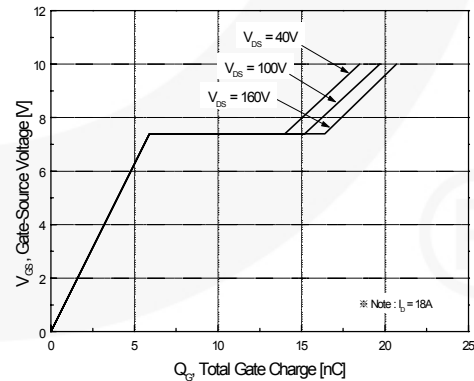


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

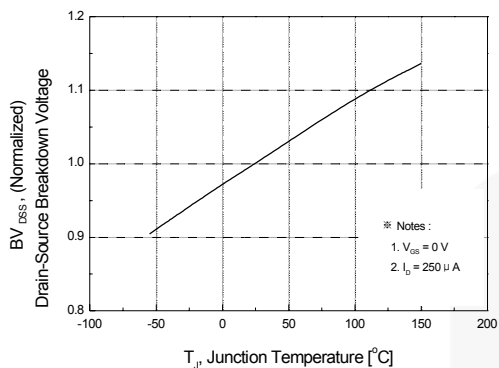


Figure 7. Breakdown Voltage Variation vs. Temperature

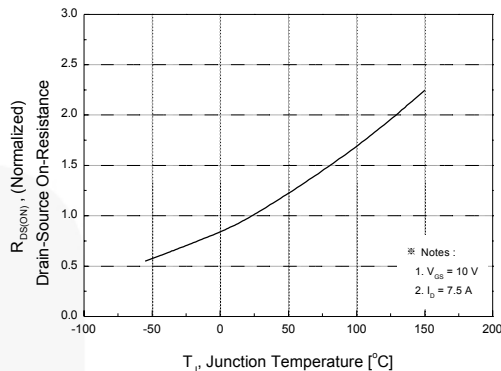


Figure 8. On-Resistance Variation vs. Temperature

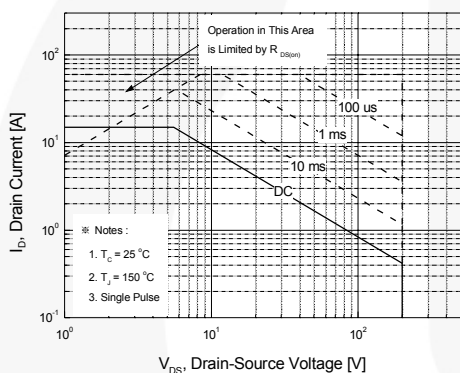


Figure 9. Maximum Safe Operating Area

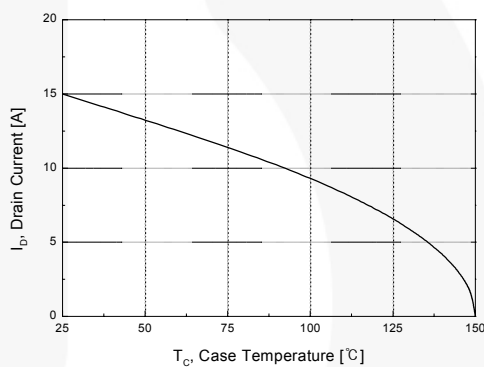


Figure 10. Maximum Drain Current vs. Case Temperature

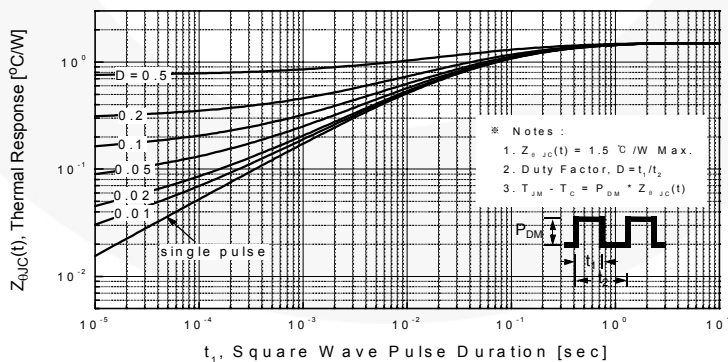


Figure 11. Transient Thermal Response Curve

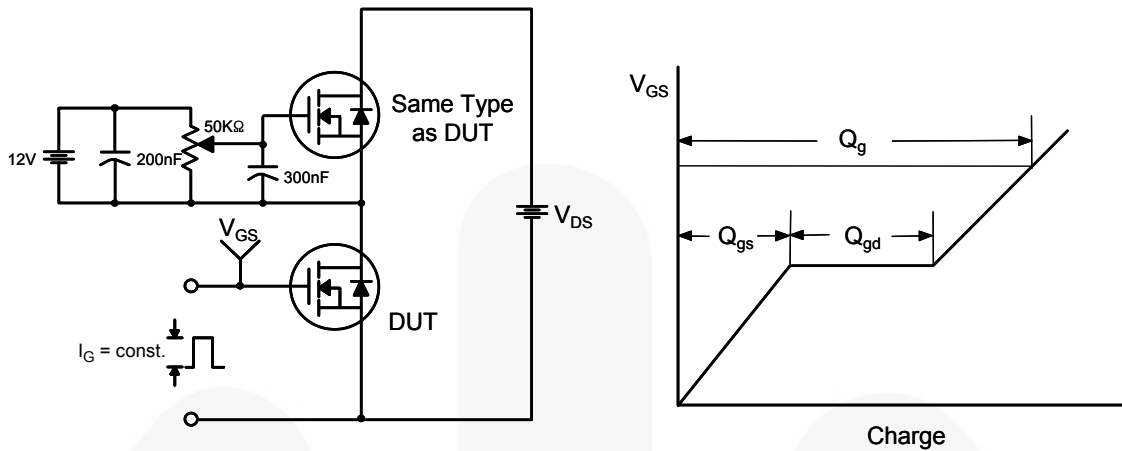


Figure 12. Gate Charge Test Circuit & Waveform

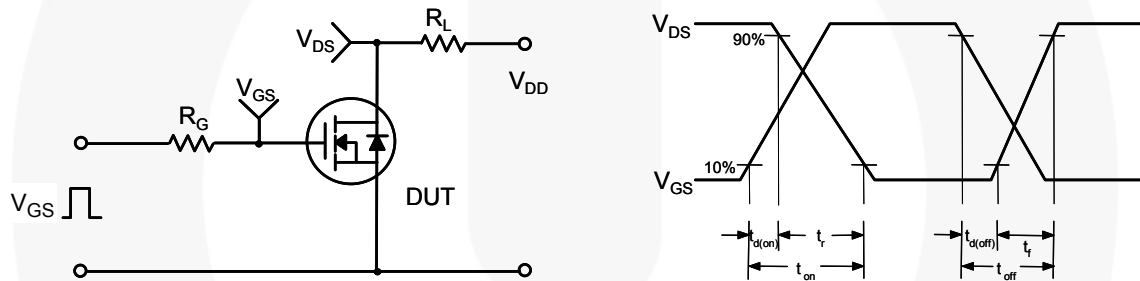


Figure 13. Resistive Switching Test Circuit & Waveforms

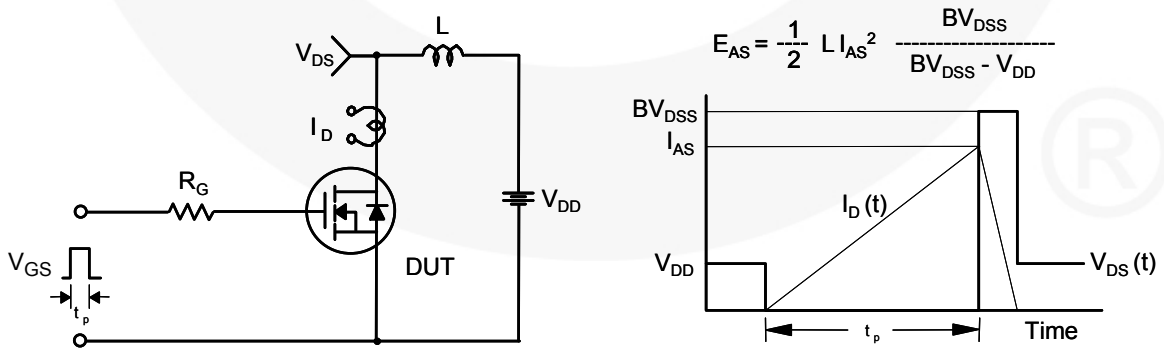


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

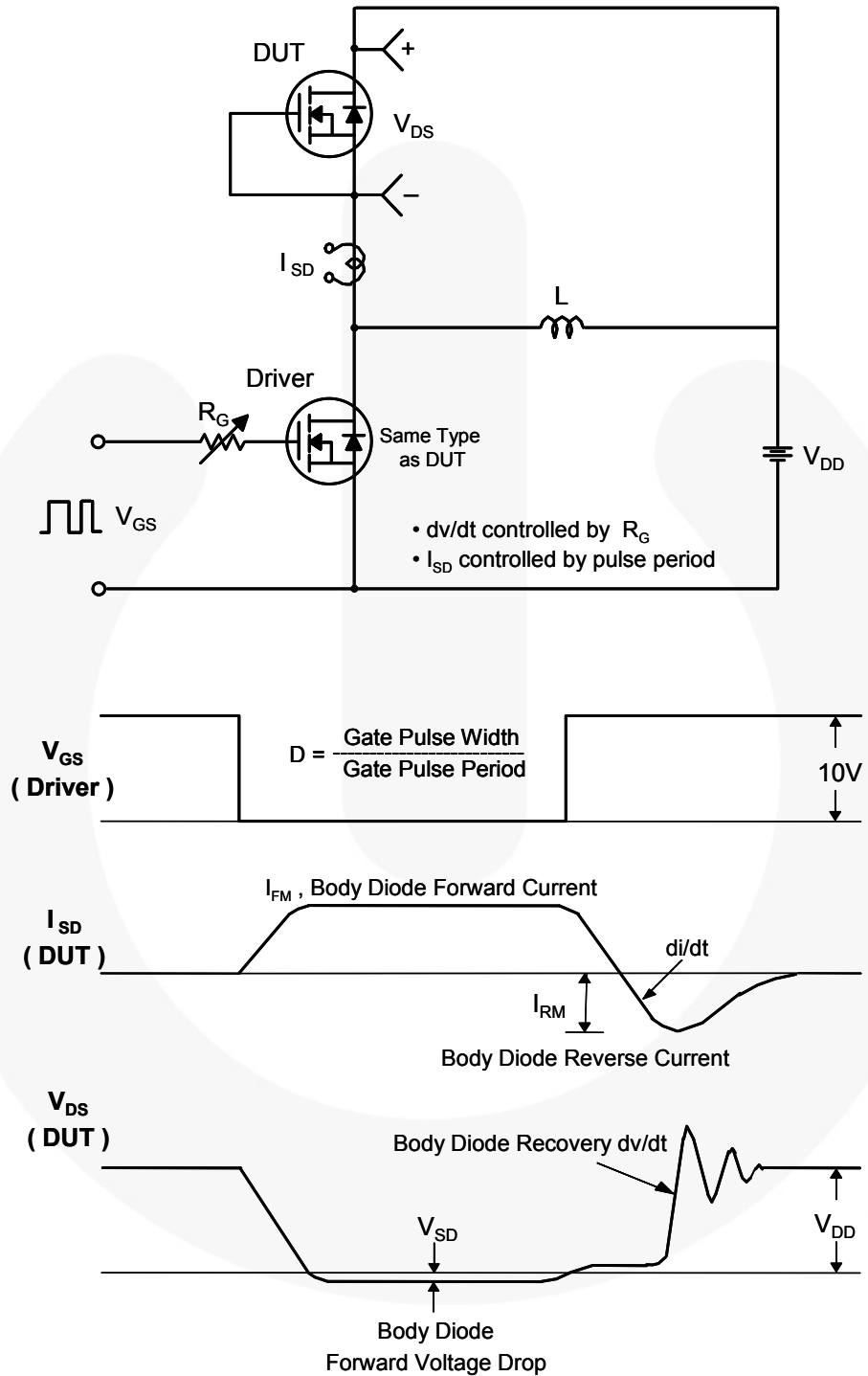
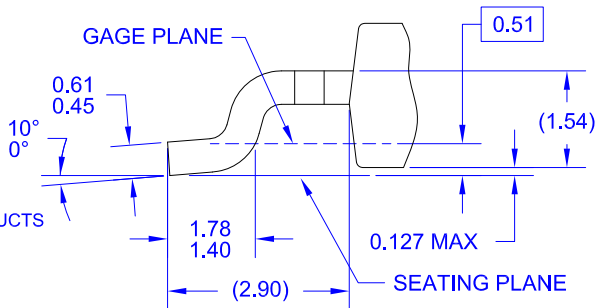


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11





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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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